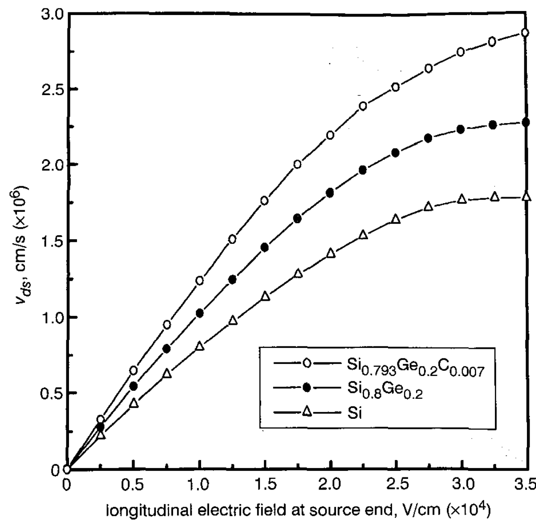

Fig. 1 *Drift velocity of holes against longitudinal electric field at source end for $Si_{0.8}Ge_{0.2}$, $Si_{0.793}Ge_{0.2}C_{0.007}$ and control Si devices*

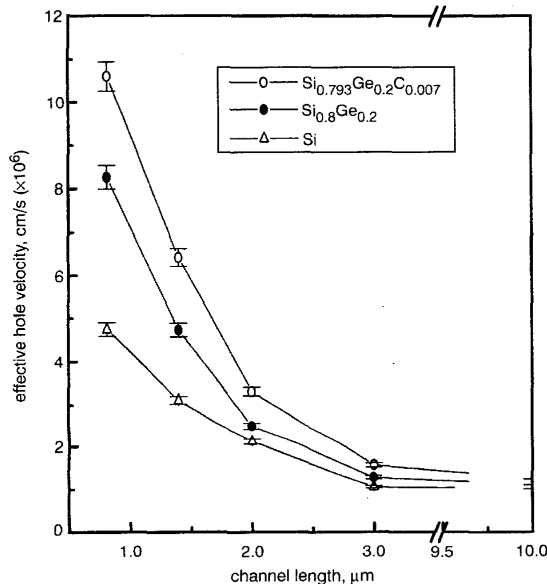

Fig. 2 *Calculated effective hole velocities against channel length of Si, $Si_{0.8}Ge_{0.2}$ and $Si_{0.793}Ge_{0.2}C_{0.007}$ inversion layers*

Study of gate length dependent effective velocity manifests the velocity overshoot effects in MOSFETs. Effective velocity of holes in control Si, $Si_{0.8}Ge_{0.2}$ and $Si_{0.793}Ge_{0.2}C_{0.007}$ devices with different channel lengths are shown in Fig. 2. As channel length decreases, v_{eff} increases in every device. In the case of the 0.8 µm device, the effective hole velocity of $Si_{0.793}Ge_{0.2}C_{0.007}$ is enhanced by 25.8% and 103% compared to $Si_{0.8}Ge_{0.2}$ and control Si devices, respectively. The value v_{eff} of holes in the control Si device is in good agreement with the reported one [7, 8]. The highest hole velocity in the $Si_{0.8}Ge_{0.2}$ *p*-MOSFET of $\sim 8 \times 10^6$ cm/s as reported by Ansaripour *et al.* [8], is comparable with our binary device data. Note the substantial increase of the effective velocity as the devices are scaled down, which may be due to the onset of hole velocity overshoot. This has also been reported by Kaya *et al.* [9], even in 1.5 µm $Si_{0.8}Ge_{0.2}$ devices. As shown in Fig. 2, the effective hole velocity of the $Si_{0.793}Ge_{0.2}C_{0.007}$ inversion layer exceeds 10^7 cm/s in the shortest channel device ($L = 0.8$ µm). This is attributed to the hole velocity overshoot [7–9], which is considerably larger in the SiGeC device compared to the SiGe and control Si MOSFETs as a result of higher mobility and longer relaxation time for holes in the strain stabilised ternary layer.

Conclusions: We have investigated the velocity-field characteristics of holes in partially strain compensated $Si_{0.793}Ge_{0.2}C_{0.007}$ *p*-MOSFET devices. The increase of high-field hole velocity in SiGeC short-channel devices in the region of non-equilibrium transport is attributed to higher mobility owing to reduced process induced strain relaxation in C-containing alloy. Therefore, in addition to the improvement of hole mobility in low-field transport, our results indicate the benefit of an early onset of velocity overshoot in short channel SiGeC devices.

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References

1 CARNS, T.K., CHUN, S.K., TANNER, M.O., WANG, K.L., KAMINS, T.I., TURNER, J.E., LIE, D.Y.C., NICOLET, M.-A., and WILSON, R.G.: 'Hole mobility measurements in heavily doped $Si_{1-x}Ge_x$ strained layers', *IEEE Trans. Electron Devices*, 1994, **41**, pp. 1273–1281

2 VERDONCKT-VANDERBROEK, S., CRABBE, E.F., MEYERSON, B.S., HARAME, D.L., RESTLE, P.J., STORK, J.M.C., and JOHNSON, J.B.: 'SiGe-channel heterojunction *p*-MOSFET', *IEEE Trans. Electron Devices*, 1994, **41**, pp. 90–100

3 OSTEN, H.J.: 'Band-gap changes and band offsets for ternary $Si_{1-x-y}Ge_xC_y$ alloys on Si(001)', *J. Appl. Phys.*, 1998, **84**, pp. 2716–2721

4 LIU, C.W., TSENG, Y.D., CHERN, M.Y., CHANG, C.L., and STURM, J.C.: 'Thermal stability of $Si/Si_{1-x-y}Ge_xC_y/Si$ quantum wells grown by rapid thermal chemical vapor deposition', *J. Appl. Phys.*, 1999, **85**, pp. 2124–2128

5 RAIS, K., GHIBAUDO, G., BALESTRA, F., and DUTOIT, M.: 'Study of saturation velocity overshoot in deep submicron silicon MOSFETs from liquid helium up to room temperature', *J. Phys. IV, Colloq. C6, Supplément au Journal de Physique III*, 1994, **4**, pp. C6-19–C6-24

6 QUINONES, E.J., JOHN, S., RAY, S.K., and BANERJEE, S.K.: 'Design, fabrication, and analysis of SiGeC heterojunction *p*-MOSFETs', *IEEE Trans. Electron Devices*, 2000, **47**, pp. 1715–1725

7 OHBA, R., and MIZUNO, T.: 'Nonstationary electron/hole transport in sub-0.1 µm MOS devices: correlation with mobility and low-power CMOS application', *IEEE Trans. Electron Devices*, 2001, **48**, pp. 338–343

8 ANSARIPOUR, G., BRAITHWAITE, G., AGAN, S., WHALL, T.E., and PARKER, E.H.C.: 'Study of velocity field characteristics in pseudomorphic $Si_{0.8}Ge_{0.2}$ *p*-channel metal-oxide-semiconductor field effect transistor', *Microelectron. Eng.*, 2000, **51–52**, pp. 541–546

9 KAYA, S., ZHAO, Y.-P., WATLING, J.R., ASENOV, A., BARKER, J.R., ANSARIPOUR, G., BRAITHWAITE, G., WHALL, T.E., and PARKER, E.H.C.: 'Indication of velocity overshoot in strained $Si_{0.8}Ge_{0.2}$ *p*-channel MOSFETs', *Semicond. Sci. Technol.*, 2000, **15**, pp. 573–578

Monolithic transformer with underlying deep silicon-oxide block

H. Jiang and N.C. Tien

A method to improve the performance of on-chip monolithic transformers is presented. A transformer with a 20 µm-deep silicon-oxide block beneath has a self-resonant frequency of 9.75 GHz and a quality factor of 10.1. These values are 72 and 124% better, respectively, than those of the same device built on 4.1 µm-thick silicon oxide.

Introduction: Monolithic transformers have found extensive applications in radio-frequency (RF) circuits such as impedance matching, signal coupling and phase splitting [1], and have been implemented in complementary metal-organic-semiconductor (CMOS) technology [1–3]. However, these transformers generally have low quality factors (*Q*s) and low self-resonant frequencies (f_{res}) [1, 3], which is in part due to the electromagnetic coupling and parasitic capacitance between the device and the lossy silicon substrate. Since spiral inductors

are typically used to form transformers, the very nature of coupling generates even more parasitic capacitance and eddy current, resulting in energy loss among each other. Therefore, to improve the performance of the on-chip monolithic transformers, the parasitics and loss due to the substrate should be suppressed as much as possible. One approach is to increase the thickness of the isolation layer, typically silicon dioxide, between the transformer and the silicon substrate. We have reported a micromachining method to form silicon-oxide blocks, up to 20 μm in thickness, in a silicon substrate at selected locations [4]. In this Letter, we demonstrate the improvement in the transformer performance when the device is fabricated on such a silicon-oxide block.

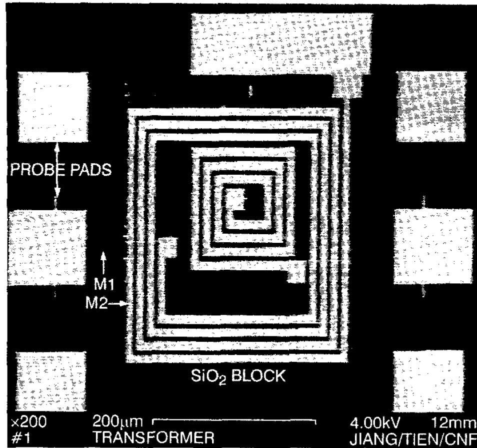

Fig. 1 *SEM image of fabricated transformer and its circuit model*

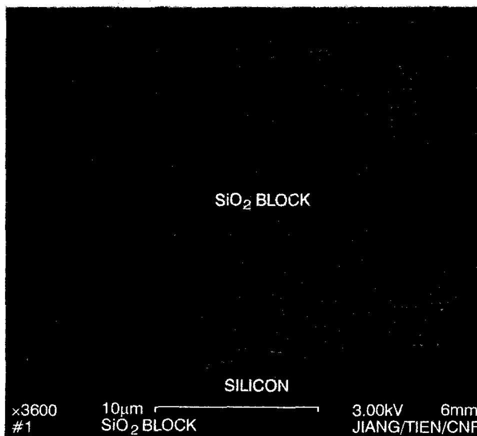

Fig. 2 *SEM image of cross-section of 20 μm-thick silicon-oxide block*

Device fabrication: A simple three-terminal transformer was fabricated at Cornell Nanofabrication Facility (CNF). Fig. 1 shows its SEM image and circuit model. The first step in its fabrication was to create a 20 μm-thick silicon-dioxide block. This was accomplished through deep reactive ion etching (DRIE) 20 μm-deep narrow beam-and-trench structures into the silicon substrate, thermal oxidation of the beams, silicon-oxide deposition to seal the gaps left after oxidation and planarisation of the surface by chemical mechanical polishing (CMP) [4]. The SEM micrograph of the silicon-oxide block is given in Fig. 2. The transformer structure was then formed, using two sputtered aluminium layers, both 1.4 μm thick, with a 1.4 μm-thick polyimide film as the insulating layer. The first aluminium layer was patterned to form underpasses that connect the input and output ports of the spirals to probe pads and ground, and the second was patterned to form the two spirals, one encompassing the other. For comparison, the same transformer was fabricated nearby without a silicon-oxide block beneath. The isolation layer between the first aluminium film and the silicon substrate was 4.1 μm-thick silicon dioxide.

Measurement results: On-wafer testing was performed on the transformers with a vector network analyser and coplanar ground-signal-ground probes. The measured two-port *S*-parameters of the transformer with the silicon-oxide block, after the deembedment of the shunt parasitics due to the probe pads, are plotted on a Smith chart as a function of frequency in Fig. 3. The inductances of the large and small spirals were calculated as 5.5 and 1.5 nH, respectively, from the measured reactances. The f_{res} of the transformer is the frequency at which one of the open-circuit input impedances, Z_{11} or Z_{22}, of the device first becomes purely resistive. Beyond this point, the device has a capacitive impedance looking into one end and no longer functions as a transformer. Two *Q*s of the transformer can be defined by the respective ratios of the reactances and resistances of Z_{11} and Z_{22}. Table 1 summarises the f_{res} and maximum Q for the two transformers, with and without the silicon-oxide block. The f_{res} is increased by 72% and the Q is increased by at least 124% with the silicon-oxide block. The coupling coefficient, k, between the two inductors was found to be 0.2. The low k is due to both the intrinsic poor confinement of the magnetic flux in a monolithic transformer of this type, including the choice of having one spiral encompassing the other. This issue can be addressed by stacking identical spiral structures if multiple metal layers are available [3].

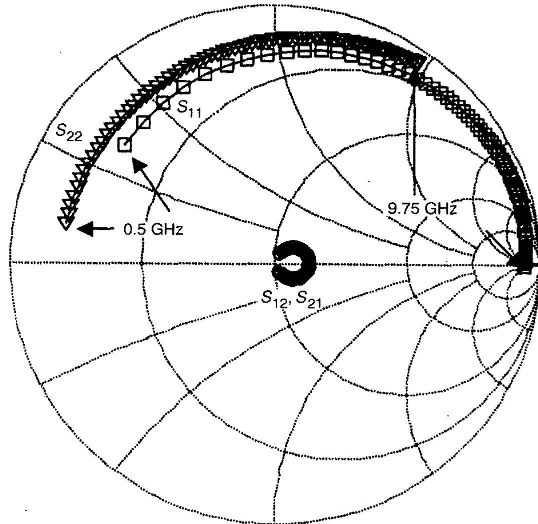

Fig. 3 *Measured S-parameters of transformer with silicon-oxide block*

Table 1: Summary of experimental results of transformers

	With SiO_2 block	Without SiO_2
Q_{max} from Z_{11}	10.1 at 4.50 GHz	4.5 at 2.0 GHz
Q_{max} from Z_{22}	20.3 at 12.38 GHz	5.7 at 7.0 GHz
f_{res} (GHz)	9.75	5.67

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References

1 ZHOU, J., and ALLSTOT, D.: 'Monolithic transformers and their application in a differential CMOS RF low-noise amplifier', *IEEE J. Solid-State Circuits*, 1998, **SC-33**, (12), pp. 2020–2027

2 LONG, J.: 'Monolithic transformers for silicon RF IC design', *IEEE J. Solid-State Circuits*, 2000, **SC-35**, (9), pp. 1368–1382

3 ZOLFAGHARI, A., CHAN, A., and RAZAVI, B.: 'Stacked inductors and transformers in CMOS technology', *IEEE J. Solid-State Circuits*, 2000, **SC-36**, (4), pp. 620–628

4 YEH, J.-L., JIANG, H., and TIEN, C.: 'Integrated polysilicon and DRIE bulk silicon micromachining for an electrostatic torsional actuator', *IEEE/ASME J. Microelectromechan. Syst.*, 1999, **MEMS-8**, (4), pp. 456–466

Small signal RF performance of AlGaN/GaN heterojunction bipolar transistors

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Small signal RF characteristics of an AlGaN/GaN HBT are presented. The devices had a short circuit current gain cutoff frequency of 2 GHz. The roll off of the short-circuit current gain (H_{21}) of the device was less than 20 dB/decade. We propose that this is due to the distributed nature of the base-collector parasitic resistance-capacitance network caused by a high sheet resistance in the base (100 kΩ/□) and high base contact resistances. Finite element small signal equivalent circuit simulations support this explanation.

Introduction: Several groups have demonstrated common emitter operation of AlGaN/GaN HBTs [1–3]. GaN is desirable for electronics applications due to saturated electron velocities of 2×10^7 cm/s [4], and its 3.4 eV bandgap which leads to a critical breakdown field of 2 MV/cm [5], and stability at high temperatures. The low conductivity of the *p*-type base material, however has caused significant problems for the DC characteristics of the AlGaN/GaN HBT [1]. In this Letter we present small signal RF characteristics of an AlGaN/GaN HBT, and discuss the effects of the low conductivity base on its performance.

Device fabrication: The device structure used for these experiments, DC device characteristics, along with the fabrication issues and difficulties associated with fabricating the DC device are discussed by McCarthy *et al.* [1]. After the DC device was fabricated, further processing was required to allow microwave testing. A Cl_2 RIE etch was used to isolate the devices from the sapphire substrate, and Cyclotene BCB was used to planarise the device structures. A blanket $CF_4 + O_2$ plasma etch was used to etch back the BCB and expose the emitter contact. Vias were then opened in the BCB exposing the base and collector contacts, and Ti/Au posts deposited. Contact pads were then deposited, completing the fabrication of the devices.

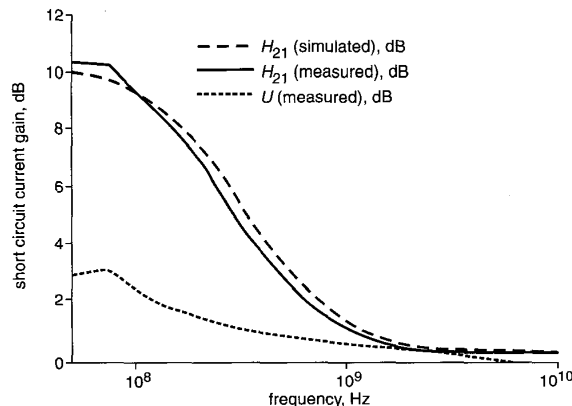

Fig. 1 *Small signal short circuit current gain (H_{21}) and Mason's unilateral gain (U) of device*

$I_c = 4$ mA. Simulated curve is small signal simulation of equivalent circuit shown in Fig. 2

Electrical characterisation: DC and RF device characterisation was performed on these devices. The DC current gain was found to be 3.5 with common emitter operation and low output conductance to 15 V. Small signal RF characterisation with a vector network analyser (VNA) from 50 MHz to 10 GHz showed agreement with DC gain measurements at 50 MHz, with a 3 dB reduction in the short circuit current gain (H_{21}) at 200 MHz and a roll off of approximately 10 dB/decade. The current gain cutoff frequency was 2 GHz, although the response with frequency became nearly flat after 1 GHz (see Fig. 1). This non-ideal behaviour of the device is thought to be due to the high sheet resistance of the base layer as well as high base contact resistances. The high resistance in the base leads to an equivalent circuit consisting of a distributed parasitic base-collector RC network which cannot be treated as a single RC time constant (Fig. 2). The result is a continuum of time constants which together lead to a reduction in H_{21} of ≅ 10 dB/decade in frequency as opposed to the ideal 20 dB/decade. To confirm the plausibility of this model, a finite element small signal equivalent circuit simulation was carried out using HP ADS. A representation of the simulated circuit is shown in Fig. 2 and the result plotted in Fig. 1. A diagram of the relevant geometries of the device is shown in Fig. 3.

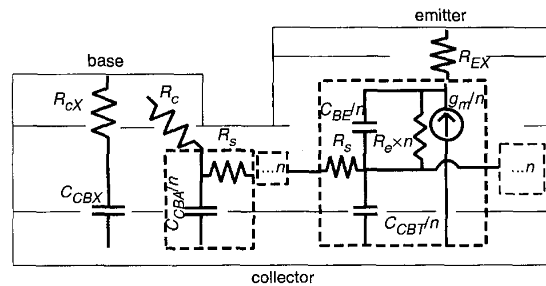

Fig. 2 *Schematic diagram of equivalent circuit of simulated circuit drawn on cross-sectional diagram of device structure*

Dashed boxes represent repeated blocks. Each block is repeated $n = 25$ times. $R_e = 3\ \Omega$

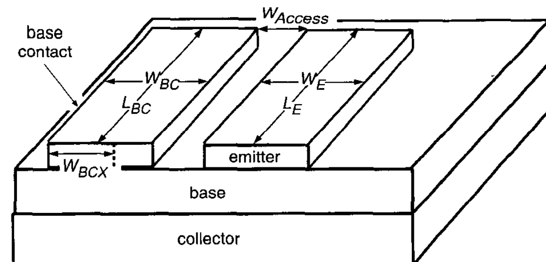

Fig. 3 *Diagram of the device geometry for AlGaN/GaN HBT and the geometry used to model the small signal RF response of the device*

Device dimensions are as follows (in microns): $W_E = 3$, $L_E = 50$, $W_{Access} = 1$, $W_{BC} = 9$, $W_{BCX} = 8$, $L_{BC} = 72$

To model the distributed nature of the device, the active and access blocks are repeated 25 times (as indicated in Fig. 2). $C_{CBX} = 0.4$ pF represents the capacitance under the extrinsic base contact, and is in series with a vertical contact resistance, $R_{cX} = 60\ \Omega$. C_{BC} also has a component in the access region to the base ($C_{CBA} = 50$ fF). Active device blocks contain a hybrid-pi small signal equivalent circuit element with a base-emitter capacitance ($C_{BE} = 0.6$ pF) and a base-collector capacitance element ($C_{CBT} = 30$ fF). The access and active blocks are connected by a sheet resistance, $R_s = 100$ kΩ/□. The small signal transconductance, g_m used was $I_E/V_T = 350$ mS, where V_T is the thermal voltage, 26 mV, and the emitter current I_E was 9 mA. The values used in the simulation represent a measured R_s in the base, I_E,