# Fabrication of Large-Area Three-Dimensional Microstructures on Flexible Substrates by Microtransfer Printing Methods

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Abstract—This paper presents two robust microtransfer printing methods, namely, multiple transfer printing and peeling microprinting methods, to fabricate three-dimensional (3-D) and high-aspect-ratio microelectromechanical systems (MEMS) structures over large areas on flexible polydimethylsiloxane (PDMS) substrates. These techniques enable conformal wrapping of 3-D microstructures, initially fabricated in two-dimensional (2-D) layouts with standard fabrication technology onto a wide range of surfaces with complex and curvilinear shapes. The processes exploit the differential adhesive tendencies of the microstructures formed between a donor and a transfer substrate to accomplish an efficient release and transfer process. Experimental and theoretical studies show that the MEMS structures with a wide variety of pattern densities can be conformally transferred to bendable device substrates while keeping the structural integrity and density intact. Quantitative stress analysis on the micromechanics of such a curvilinear system suggests that the stress induced by wrapping the complete structure onto a cylinder is mostly in the flexible PDMS substrate, while the MEMS structures experience little stress. [2011-0260]

*Index Terms*—Flexible substrates, high aspect ratio, nonplanar surfaces, peeling microprinting method, three-dimensional (3-D) microstructures, transfer printing.

#### I. INTRODUCTION

M ICROELECTROMECHANICAL systems (MEMS) and electronics fabricated over large area on nonplanar substrates with bendable and conformal features have drawn great attention in the past two decades for its versatility and functionality [1]–[3]. They have been extensively employed in a wide range of applications such as flexible display, electronic textiles, sensory skins, artificial muscle, radio frequency (RF) tags, optical MEMS, conformal X-ray imagers, health

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monitoring devices, and electronic eye cameras [4]-[14]. However, these types of systems generally require specific fabrication technologies very different from the established microfabrication techniques due to the restriction of the inherently planar nature of lithography, etching, doping, and material growth [15]. In addition, with plastics being the widely accepted substrates for flexible electronics, another technological challenge inevitably ensues, i.e., forming highquality MEMS and electronic devices with single-crystal silicon (Si) on plastic substrates needs thermal processes exceeding the glass-transition or thermal decomposition temperatures of plastics [16]. To address these issues, other alternatives to implement micro-/nanodevices on flexible substrates have been widely explored in recent years, including laser lithography on nonplanar surfaces [17], [18], stressassisted elastomeric stamp [19], self-assembly [20], direct machining [21], [22], and flexible mask on a cylindrical surface [3]. Unfortunately, the thickness of the device structures by these techniques is limited up to 2  $\mu$ m, which is enough for electronic devices but unfavorably constrains the applications of 3-D MEMS and photonic devices.

We previously reported preliminary results on a transfer technique to circumvent the aforementioned limitations in processing while maintaining flexible and conformal features of the substrate [23], [24]. Here, we present expanded works on the development of fabrication techniques to produce large-area high-aspect-ratio MEMS structures conformally formed onto flexible substrates with curvilinear surfaces. Specifically, we report on two robust microtransfer printing methods-multiple transfer printing and peeling microprinting methods. These transfer techniques rely primarily on the disparate adhesive tendencies of the microstructures formed between a donor substrate and a transfer substrate. For an effective delivery to occur, differential adhesion must be present so that the relative adhesive strength at the interface between the object and the transfer substrate is higher than that between the object and donor substrate [25]. In our multiple transfer printing process, for example, the 3-D high-aspect-ratio MEMS structures patterned on a silicon-on-insulator (SOI) wafer is first transferred to a photoresist AZ4620-coated polyethylene terephthalate (PET) thin film via selective undercut etching by buffered oxide etch (BOE) solution. The attachment between the microstructures and the supporting SOI wafer is significantly loosened as the BOE solution gradually removes the buried oxide (BOX) layer under the microstructures. Here, the AZ4620-coated PET thin film only serves as an intermediate transfer substrate. The MEMS structures partially embedded in AZ4620 substrate is then attached to a flexible destination substrate with a more arbitrary surface contour, e.g., a polydimethylsiloxane (PDMS) membrane. Differential adhesion favoring the bonding between the microstructures and PDMS is formed as the ultraviolet (UV)-sensitive AZ4620 decomposes during flood exposure and subsequent acetone rinse. Similarly, the peeling microprinting process takes advantage of the peeling force exerted in the lateral direction to break the bonding between the object and the donor substrate for the realization of a complete delivery to the destination substrate.

These two techniques are capable of transferring 3-D highaspect-ratio MEMS structures that cover large areas onto almost any flexible substrates. There are a number of major technological advantages over other existing transfer techniques. First, no stress-assisted stamping is required, thus greatly reducing the complexity of the release and transfer process. Second, throughput and yield can be improved since the entire device fabrication is compatible with microelectronics fabrication infrastructure. In addition, with the success of multiple transfers, all of the fabrication procedures for the MEMS, microelectronics, and photonic devices by the "top-down approach" can be implemented prior to the transfer process to prevent thermal degradation of the plastic substrate. Above all, this transfer process may provide a practical route to assembling separately fabricated devices and/or materials onto a common flexible substrate in a highly controlled fashion that is cost effective and scalable to large areas, potentially tens of square centimeters.

## II. FABRICATION

### A. Multiple Transfer Printing Method

Fig. 1 schematically shows the fabrication process flow of the multiple transfer printing technique, starting with the preparation of a donor substrate with large-area organized arrays of 3-D high-aspect-ratio Si pillar structures on an SOI wafer. The SOI wafer (Silicon Quest International, Inc., Santa Clara, CA) has 60- $\mu$ m-thick Si and 2- $\mu$ m-thick BOX layers, as shown in Fig. 1(a). First, a silicon-dioxide  $(SiO_2)$  layer of 800 nm in thickness is thermally grown by wet oxidation at 1050 °C for 2 h. Positive photoresist Shipley 1813 (MicroChem Corp., MA) of 2  $\mu$ m in thickness is spun and photo-patterned via standard contact-mode lithography, as shown in Fig. 1(b). Next, the SiO<sub>2</sub> layer is etched in 6:1 BOE solution for 10 min, as shown in Fig. 1(c). The Si layer is then etched using inductively coupled plasma (ICP) deep reactive ion etching (DRIE; Surface Technology Systems, Newport, U.K.) for 1 h to form high-aspectratio Si pillar arrays, as shown in Fig. 1(d). Here, both SiO<sub>2</sub> layer and photoresist (PR) serve as hard masks, while the BOX laver functions as an etch-stop laver for the DRIE process. The etching process consists of two distinctive fabrication cycles-a passivation cycle and an etching cycle. Each passivation cycle lasts for 6 s, and the gas flow of octafluorocyclobutane  $(C_4F_8)$ is 12 standard cubic centimeters per minute (sccm). The power on RF coil and RF platen are 600 and 0 W, respectively. On the other hand, each etching cycle is 11 s. The gas flows



Fig. 1. Fabrication process flow of a Si pillar array fabricated on a flexible PDMS substrate by a multiple transfer printing method. (a) An SOI wafer of two layers of 60- $\mu$ m-thick Si and 2- $\mu$ m-thick BOX layer is used as a donor substrate. (b) A SiO<sub>2</sub> layer of 800 nm is thermally grown at 1050 °C for 2 h, and patterning is achieved by the standard contact-mode photolithography. (c) Top SiO<sub>2</sub> hard mask is wet etched in a 6:1 BOE solution for 10 min. (d) Si is anisotropically etched by ICP DRIE for 1 h to form a pillar array with BOX layer as an etch-stop layer. (e) SiO<sub>2</sub> hard mask and the BOX layers are removed in a 6:1 BOE solution. Precise time-controlled undercut etching of BOX is required and dependent upon the Si pillar density. The BOX layer is etched to a level that the silicon pillars are only loosely attached to the SOI wafer. (f) AZ4620-coated PET is attached to the pre-etched SOI wafer and baked at 110 °C for 10 min to cure the PR and to strengthen the interfacial adhesion between the Si pillar array and AZ4620. (g) Transfer and release step is accomplished by immersing the whole device in the 6:1 BOE solution for 10 min to thoroughly transfer the Si pillar arrays from the SOI wafer onto the AZ4620-coated PET substrate. Here, (a)-(g) represent the first transfer. (h) PDMS with 10:1 mass ratio of silicone elastomer and the curing agent are spun onto a fresh PET thin film. (i) Pressing the PDMS against the Si pillar arrays and baking at 80 °C for 2 h are followed by the removal of the PET sheet from PDMS. (j) Flood exposure to AZ4620 for 20 min to decrosslink the polymer chains is performed. (k) Entire device is then immersed in an acetone solution for 12 h to thoroughly remove the PR residues. (1) With the completion of the second transfer process, the Si pillar arrays are successfully transferred to the bendable PDMS membrane that can deform to almost any curvilinear shape

of sulfur hexafluoride  $(SF_6)$  and oxygen  $(O_2)$  are 130 and 13 sccm, respectively. The power on RF coil and RF platen are 600 and 13 W, respectively [23]. Next, the entire donor substrate is dipped in the BOE solution to perform selective undercut etching of the BOX layer to a level that the Si pillar microstructures are only loosely attached to the supporting SOI wafer, as shown in Fig. 1(e). This etching step requires precise control of time, which is 90, 100, 105, and 110 min in our experiments for four different pattern densities, namely, 3.8, 6.7, 15, and 60 pillars per mm<sup>2</sup>, respectively. The etching behavior generally follows the trend that lower pattern density (i.e., larger interpillar spacing) requires a shorter wet etching time due to higher accessibility of the BOE solution to the BOX layer. Subsequently, another type of positive photoresist AZ4620 (AZ Electronic Materials, Somerville, NJ) is spin-coated onto a UVtransparent PET with 76  $\mu$ m in thickness (Melinex ST505, DuPont Teijin Films, Wilmington, DE), which now operates

as an intermediate transfer substrate. The AZ4620-coated PET is later attached to the pre-etched SOI wafer and is baked at 110 °C for 10 min to cure the photoresist and to strengthen the interfacial adhesion between the Si pillar array and AZ4620, as shown in Fig. 1(f). The transfer and release step is performed by immersing the whole device into the 6:1 BOE solution for 10 min to completely transfer the Si pillar arrays from SOI wafer onto the AZ4620-coated PET substrate, shown in Fig. 1(g). Unlike the conventional release and transfer process applied in other transfer printing methods, an additional timecontrolled pre-etching by BOE solution is previously employed to facilitate the release step due to the vulnerability of AZ4620 to the BOE solution [24]. So far, Fig. 1(a)-(g) shows the first transfer process. The second transfer can be implemented by utilizing materials with transparent, structurally robust, and bendable features, e.g., PDMS. The preparation of PDMS starts with Sylgard 184 (Dow Corning Corp., Midland, MI), a silicone elastomer kit containing the base (i.e., elastomer) and the curing agent. They are mixed in 10:1 mass ratio to crosslink into PDMS and then put in a vacuum chamber for 1 h to remove the trapped air bubbles. It should be noted that even a small number of air bubbles can severely affect both the mechanical and optical properties of the PDMS membrane. Next, the solution is spin-coated onto the PET to form a PDMS thin film of 500  $\mu$ m in thickness as the final device substrate, as shown in Fig. 1(h). After pressing the thin film against the Si pillar arrays on AZ4620 and baking at 80 °C for 2 h, PET is peeled off from the PDMS, as shown in Fig. 1(i). Preferential adhesion is formed at the interface between the Si pillar arrays and the PDMS by decrosslinking the UV-sensitive AZ4620 with flood exposure for 20 min, as shown in Fig. 1(j). The entire device is then immersed in an acetone solution (Fisher Scientific, Fair Lawn, NJ) for 12 h to thoroughly remove the PR residues, as shown in Fig. 1(k). After detaching from the intermediate transfer substrate, the Si pillar arrays are successfully transferred to the bendable and conformal PDMS substrate that can deform to almost any curvilinear shape, as shown in Fig. 1(1). The main advantage of this approach as compared to the peeling microprinting method described in the following is that it allows for transferring of MEMS structures onto any flexible substrate through the multiple-step transfer.

# B. Peeling Microprinting Technique

In addition to the multiple transfer printing technique, an alternative microtransfer printing process without the need of an intermediate transfer substrate has also been successfully developed. The patterning of 3-D high-aspect-ratio Si pillar structures on an SOI wafer and the time-controlled pre-etching by the BOE solution to create differential adhesion are the same, as shown in Fig. 1(a)–(e). Similarly, the pre-etching process performs precise undercut etching to leave the pillar structures loosely attached and thereby forms the bonding favoring the adhesion between the PDMS and the MEMS structures. Here, instead of utilizing the AZ4620, a PDMS membrane which serves as the final device substrate is employed to directly transfer the MEMS structures. The main difference from the previous method lies in the fact that we can easily deliver

Fig. 2. SEM images of the Si pillar arrays after DRIE. The height of all pillars is defined by the silicon layer to be 60  $\mu$ m. SEM images of different pillar densities of (a) 60, (b) 15, (c) 6.7, and (d) 3.8 pillars per mm<sup>2</sup>, each corresponding to an interpillar spacing of 50, 100, 150, and 200  $\mu$ m, respectively.

the microstructures onto PDMS by quickly peeling off the flexible membrane. The fast peeling exerts sufficiently large shear force to break weak linkages between the pillar arrays and the supporting SOI wafer. The primary advantages of the peeling microprinting method over the multiple transfer printing are as follows. First, since the release and transfer process does not contact PDMS with the BOE solution, it can remain structurally intact and optically transparent, which could benefit some applications such as flexible display. Second, this process only requires one-step direct stamping of the PDMS membrane to the objects (i.e., Si pillar arrays) without an intermediate transfer substrate; hence, an increased throughput can be expected.

#### **III. EXPERIMENTAL RESULTS**

#### A. Process Yield Assessment

Different pattern densities of the 3-D high-aspect-ratio Si pillar arrays are designed and implemented to assess the efficacy and yield of both the multiple transfer printing and peeling microprinting methods. Fig. 2 shows the scanning electron microscope (SEM) images of pillar arrays of four pattern densities etched by DRIE. The pillar densities are 60, 15, 6.7, and 3.8 pillars per  $mm^2$ , respectively, with each corresponding to an interpillar spacing of 50, 100, 150, and 200  $\mu$ m, respectively. The height of all pillars is approximately the same as the thickness of the Si layer of the SOI wafer, which is 60  $\mu$ m. The widths of the outside and inside squares are 100 and 50  $\mu$ m, respectively. The images provide a clear evidence that the 3-D high-aspect-ratio pillars with vertical sidewalls have been achieved by the highly anisotropic etching. The maintenance of pattern density and structural integrity of the MEMS structures after the transfer are key indicators to assess the efficacy and yield of the two transfer methods. From the micro-/nanoelectronics perspectives, the higher the deviation from the pattern designs of the layouts is, the greater degradation





Fig. 3. Top view OM images of the Si pillar arrays after being delivered from the AZ4620/PET thin film onto the PDMS membrane by the multiple transfer printing method. Structures with four different pattern densities, namely, (a) 60, (b) 15, (c) 6.7, and (d) 3.8 pillars per mm<sup>2</sup>, respectively, are all successfully transferred.

in device performance and process yield may result. In this case, the 3-D high-aspect-ratio Si pillar arrays with vertical and smooth sidewall profiles have great potentials in optical MEMS and photonic applications. Therefore, the consistency between the posttransfer periodicity of the pillar arrays and the layout design is of paramount significance. In our experiments, after being delivered to the PDMS substrate from AZ4620/PET thin film via the multiple transfer printing technique, the pattern density of the microstructures partially enclosed in the flexible membrane remains unchanged based on the results of both optical microscopic (OM) and SEM images, as shown in Figs. 3 and 4, respectively. Similar results are also obtained in the peeling microprinting method, as shown in Fig. 5. In Figs. 3-5, (a)-(d) represent densities of 60, 15, 6.7, and 3.8 pillars per mm<sup>2</sup>, respectively, in alphabetical order. It should be noted that the surface roughness of the PDMS substrate can be improved when implementing a precuring treatment at 80 °C for 3 min as shown in (c) and (d) of both Figs. 4 and 5, as compared to (a) and (b) where the treatment was not applied. In addition, maintaining structural integrity is also considered critical, especially for photonic and MEMS devices because damage to the microstructures during processing can either induce undesirable changes in the optical and mechanical properties, or worse, failure of the device. Fig. 6 shows the capability of the flexible PDMS membrane to undergo larger deformation under an external stress without structural failure. Fig. 6(a) shows OM images of the Si pillar arrays on the flexible PDMS substrate under bending. The PDMS membrane can also be attached and conformed to a hemispherical dome with a diameter of 32 mm, as shown in Fig. 6(b). Fig. 7 shows the SEM images of the PDMS membrane wrapped onto objects with curvilinear surfaces. Wrapping of the PDMS thin film



Fig. 4. Top view SEM images of the Si pillar arrays after being delivered from the AZ4620/PET thin film onto the PDMS membrane by the multiple transfer printing method.



Fig. 5. Top view SEM images of the Si pillar arrays after being delivered from the SOI wafer onto the PDMS membrane by the peeling microprinting method. All structures with four different pattern densities, namely, (a) 60, (b) 15, (c) 6.7, and (d) 3.8 pillars per mm<sup>2</sup>, respectively, are successfully transferred.

on a hemispheric shell with a diameter of 18.2 mm and a cylinder with a diameter of 16 mm are shown in Fig. 7(a) and (b), respectively. It should be noted that, even under large deformation, the PDMS membrane, which serves as a device substrate, still exhibits excellent physical properties such as bendable and conformal features without cracking.

For the actual yield of the microtransfer printing methods, our empirical estimation of the average success rate of transfer is about 70% (14 times of successful transfers out of 20 experiments in total). The success rate of transfer is defined as



Fig. 6. OM images of the flexible PDMS membrane partially embedded with Si pillar arrays (a) under bending, (b) attached, and conformed to a hemisphere with a diameter of 32 mm.



Fig. 7. SEM images of the PDMS membrane partially embedded with Si pillar arrays when (a) attached to the surface of a hemispheric shell with a diameter of 18.2 mm and (b) wrapped onto a cylindrical object with a diameter of 16 mm.

when more than 80% of all the microstructures in the patterned area are effectively transferred from the donor substrate to the PDMS membrane.

#### B. Process Improvement for Conformal Adhesion

During the transfer process, pressing a soft elastomeric transfer substrate against solid objects does not necessarily lead to conformal contact at each interface, especially when the surface area of the object is too large to form uniform contact or the pressure exerted is not uniform across the entire surface. This nonuniform adhesive stamping behavior may lead to issues such as uneven height distribution of the pillar structures on the PDMS surface and/or excessive residual stress concentrated at the corner of the pillars, etc. These problems are very likely to plague potential applications such as optical reflecting mirrors. Fig. 8(a) shows another issue, where undesired concave dimples are present at the bottom of the Si pillars. To address these problems, we have found that increasing the hardness of the PDMS substrate by a precuring treatment at 80 °C for 3 min prior to contacting the objects (i.e., Si pillars) can facilitate conformal adhesion between interfaces, as shown in Fig. 8(b). The mechanism can be explained as that the PDMS with increased hardness becomes less susceptible to the nonuniform pressure applied during contact but still possesses sufficient adhesion required for a successful transfer. In Fig. 8(a) and (b), SEM images of Si pillar arrays partially embedded in the PDMS membrane, respectively, without and with precuring treatment at 80 °C for 3 min prior to the peeling microprinting process clearly indicate complete removal of the concave dimples and thus a much improved height distribution uniformity of the pillar arrays on the PDMS substrate.



Fig. 8. SEM images of Si pillar arrays partially embedded in the PDMS membrane (a) without and (b) with precuring treatment at 80 °C for 3 min prior to the peeling microprinting process. These images clearly suggest that the precuring treatment can significantly remove the concave dimples at the bottom of the pillars and thus improves the height distribution uniformity of the pillar arrays on the PDMS substrate.



Fig. 9. Quantitative analysis by ANSYS on the stress distribution within the PDMS membrane partially embedded with Si pillar arrays when wrapped onto a cylinder with a diameter of 1 mm. The thickness of the PDMS membrane is 20  $\mu$ m. The height of the Si pillar is 55  $\mu$ m above the surface, with a penetration depth of 5  $\mu$ m inside the membrane. Most stress is distributed within the PDMS membrane, and the Si pillar structures experience little stress.

### C. Stress Analysis by ANSYS Simulation

Good mechanical flexibility of the device is considered as a critical feature of many of the envisioned applications described previously in Section I. An analysis on stress distribution within a thin film can provide valuable insights for the detailed investigation on mechanics such as mechanical failure models and locations of the stress concentration under large deformation. Here, a quantitative stress analysis based on a 3-D finite-element method is performed by commercial software ANSYS (ANSYS 12.1 Release, ANSYS, Inc., Canonsburg, PA) to simulate the wrapping behavior of a flexible PDMS membrane partially embedded with Si pillar arrays onto a cylinder with a diameter of 1 mm, as shown in Fig. 9. Due to axial symmetry, a  $4 \times 4$  pillar array is sampled in ANSYS for simplicity. Symmetric boundary conditions are applied to corresponding surfaces to improve the simulation accuracy. Parameters set for modeling are as follows: structural material I (PDMS): Young's modulus of 750 kPa and Poisson ratio of 0.49; structural material II (single crystal Si): Young's modulus of 150 GPa and Poisson ratio of 0.17. The thickness of the PDMS membrane is set to be as thin as 20  $\mu$ m. The height of the Si pillar is 55  $\mu$ m above the surface, with a penetration depth of 5  $\mu$ m within the membrane. Stress distribution analysis is shown in Fig. 9. To accomplish the comprehensive simulation, we match each meshing grid point to cylindrical coordinates corresponding to a cylinder rod with a diameter of 1 mm. Based on the simulation results, the stress within the PDMS membrane while wrapping onto the cylindrical body has a maximum of 70.3 kPa, which is much lower than the fracture strength of PDMS (2.24 MPa). Most stress is present in the PDMS membrane, while the Si pillar structures experience little stress. Stress concentration points near the interfaces of two heterogeneous materials can greatly reduce the adhesion. In this case, no sign of stress concentration around the corner of the Si pillars is observed. The simulation results are consistent with our previous observations in Figs. 6 and 7 that no structural defects or related mechanical failures are found in deformed PDMS membranes. More importantly, we can conclude that low-stress conformal wrapping of the PDMS membrane on any curvilinear surfaces can be accomplished. Slightly wavy or uneven sides of the membrane are present due to a few asymmetrical meshing points lining up on both sides, which are far away from the area of interest, i.e., the pillar arrays, and thereby, they will not affect the main results of and the conclusion drawn from the analysis.

We also estimated the maximum critical stress exerted in the PDMS based on our empirical study. The minimum radius of curvature of our device under bending without fracture is about 1.2 mm. Parameters for calculations are listed as follows: Young's modulus of PDMS: 750 kPa; Poisson ratio of PDMS: 0.49. Thicknesses of PDMS and Si are 500 and 60  $\mu$ m, respectively. Based on ANSYS simulation similar to that described previously, the maximum stress in the PDMS membrane is about 2.1 MPa. It should be noted that it is a strongly materialdependent estimation, so it may only apply to this specific case.

#### **IV. CONCLUSION**

In summary, we have demonstrated two robust and efficient methods, namely, multiple transfer printing and peeling microprinting processes, to fabricate 3-D high-aspect-ratio MEMS structures onto flexible elastomeric substrates over a large area. These structures were initially patterned in 2-D layouts with standard fabrication technology and then transferred to the ultimate flexible substrates. Both techniques rely primarily on differential adhesion of the microstructures between a donor and a transfer substrate to facilitate a complete release and transfer process. Si pillar arrays with four different pattern densities were successfully transferred to flexible PDMS membranes with high yield and throughput. Both OM and SEM images show that structural integrity and pillar density were well maintained after the transfer process. No cracking or any other related mechanical failures were observed when the PDMS membrane underwent large deformation such as bending and intimately adhered to a hemispherical dome. In addition, a quantitative analysis by ANSYS to simulate the wrapping behavior of the PDMS membrane on a cylinder indicates that the stress is mostly in the flexible substrate and that the pillar structures experience little stress. The maximum stress induced is much lower than the fracture strength of the PDMS. The experimental results reaffirm the feasibility of the conformal wrapping on objects with curvilinear surfaces. These processing techniques could enable transferring of largearea MEMS structures and functional devices and modules to any nonplanar surfaces involving heterogeneous materials, thus possessing great potential in MEMS, electronic, optoelectronic, and photonic systems. In the future, we intend to enhance the versatility and functionality of our microtransfer printing methods by adding the capability to form flexible electrical conductors to interconnect active devices [26] so that highaspect-ratio MEMS structures can be completely integrated with electronics onto flexible substrates. Such technology platform could enable many novel devices with more or higher functionalities, such as 3-D microoptical imaging systems [27]. In addition, we will continue on the study and measurement of minimum peeling force required to achieve complete transfer of devices with various pattern densities, as well as the in-film stress in the devices.

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#### REFERENCES

- Y. G. Sun and J. A. Rogers, "Inorganic semiconductors for flexible electronics," *Adv. Mater.*, vol. 19, no. 15, pp. 1897–1916, Aug. 2007.
- [2] K. Bock, "Polymer electronics systems—Polytronics," Proc. IEEE, vol. 93, no. 8, pp. 1400–1406, Aug. 2005.
- [3] W. J. Li, J. D. Mai, and C. M. Ho, "Sensors and actuators on nonplanar substrates," *Sens. Actuators A, Phys.*, vol. 73, no. 1/2, pp. 80–88, Mar. 1999.
- [4] R. H. Reuss, B. R. Chalamala, A. Moussessian, M. G. Kane, A. Kumar, D. C. Zhang, J. A. Rogers, M. Hatalis, D. Temple, G. Moddel, B. J. Eliasson, M. J. Estes, J. Kunze, E. S. Handy, E. S. Harmon, D. B. Salzman, J. M. Woodall, M. A. Alam, J. Y. Murthy, S. C. Jacobsen, M. Olivier, D. Markus, P. M. Campbell, and E. Snow, "Macroelectronics: Perspectives on technology and applications," *Proc. IEEE*, vol. 93, no. 7, pp. 1239–1256, Jul. 2005.
- [5] P. F. Baude, D. A. Ender, M. A. Haase, T. W. Kelley, D. V. Muyres, and S. D. Theiss, "Pentacene-based radio-frequency identification circuitry," *Appl. Phys. Lett.*, vol. 82, no. 22, pp. 3964–3966, Jun. 2003.
- [6] C. J. Drury, C. M. J. Mutsaerts, C. M. Hart, M. Matters, and D. M. de Leeuw, "Low-cost all-polymer integrated circuits," *Appl. Phys. Lett.*, vol. 73, no. 1, pp. 108–110, Jul. 1998.
- [7] A. Nathan, B. Park, A. Sazonov, S. Tao, I. Chan, P. Servati, K. Karim, T. Charania, D. Striakhilev, Q. Ma, and R. V. R. Murthy, "Amorphous silicon detector and thin film transistor technology for large-area imaging of X-rays," *Microelectron. J.*, vol. 31, no. 11/12, pp. 883–891, Dec. 2000.
- [8] F. Axisa, P. M. Schmitt, C. Gehin, G. Delhomme, E. McAdams, and A. Dittmar, "Flexible technologies and smart clothing for citizen medicine, home healthcare, and disease prevention," *IEEE Trans. Inf. Technol. Biomed.*, vol. 9, no. 3, pp. 325–336, Sep. 2005.
- [9] H. C. Ko, M. P. Stoykovich, J. Z. Song, V. Malyarchuk, W. M. Choi, C. J. Yu, J. B. Geddes, J. L. Xiao, S. D. Wang, Y. G. Huang, and J. A. Rogers, "A hemispherical electronic eye camera based on compressible silicon optoelectronics," *Nature*, vol. 454, no. 7205, pp. 748–753, Aug. 2008.
- [10] D.-H. Kim, N. Lu, R. Ma, Y.-S. Kim, R.-H. Kim, S. Wang, J. Wu, S. M. Won, H. Tao, A. Islam, K. J. Yu, T.-i. Kim, R. Chowdhury, M. Ying, L. Xu, M. Li, H.-J. Chung, H. Keum, M. McCormick, P. Liu, Y.-W. Zhang, F. G. Omenetto, Y. Huang, T. Coleman, and J. A. Rogers, "Epidermal

electronics," Science (New York), vol. 333, no. 6044, pp. 838-843, Aug. 2011.

- [11] Y. Xu, Y. C. Tai, A. Huang, and C. M. Ho, "IC-integrated flexible shearstress sensor skin," *J. Microelectromech. Syst.*, vol. 12, no. 5, pp. 740–747, Oct. 2003.
- [12] M. Yano, F. Yamagishi, and T. Tsuda, "Optical MEMS for photonic switching-compact and stable optical crossconnect switches for simple, fast, and flexible wavelength applications in recent photonic networks," *IEEE J. Sel. Topics Quantum Electron.*, vol. 11, no. 2, pp. 383–394, Mar./Apr. 2005.
- [13] Y. Xu, F. Jiang, S. Newbern, A. Huang, C. M. Ho, and Y. C. Tai, "Flexible shear-stress sensor skin and its application to unmanned aerial vehicles," *Sens. Actuators A, Phys.*, vol. 105, no. 3, pp. 321–329, Aug. 2003.
- [14] S. Tung, S. R. Witherspoon, L. A. Roe, A. Silano, D. P. Maynard, and N. Ferraro, "A MEMS-based flexible sensor and actuator system for space inflatable structures," *Smart Mater. Struct.*, vol. 10, no. 6, pp. 1230–1239, Dec. 2001.
- [15] H. C. Ko, G. Shin, S. D. Wang, M. P. Stoykovich, J. W. Lee, D. H. Kim, J. S. Ha, Y. G. Huang, K. C. Hwang, and J. A. Rogers, "Curvilinear electronics formed using silicon membrane circuits and elastomeric transfer elements," *Small*, vol. 5, no. 23, pp. 2703–2709, Dec. 2009.
- [16] R. A. Street, "Thin-film transistors," Adv. Mater., vol. 21, no. 20, pp. 2007–2022, May 2009.
- [17] M. Mizoshiri, H. Nishiyama, J. Nishii, and Y. Hirata, "Silica-based microstructures on nonplanar substrates by femtosecond laser-induced nonlinear lithography," *J. Phys., Conf. Ser.*, vol. 165, no. 1, p. 012048, Jun. 10, 2009.
- [18] D. Radtke and U. D. Zeitner, "Laser-lithography on non-planar surfaces," Opt. Exp., vol. 15, no. 3, pp. 1167–1174, Feb. 5, 2007.
- [19] M. A. Meitl, Z. T. Zhu, V. Kumar, K. J. Lee, X. Feng, Y. Y. Huang, I. Adesida, R. G. Nuzzo, and J. A. Rogers, "Transfer printing by kinetic control of adhesion to an elastomeric stamp," *Nat. Mater.*, vol. 5, no. 1, pp. 33–38, Jan. 2006.
- [20] F. Gholamrezaie, S. G. J. Mathijssen, E. C. P. Smits, T. C. T. Geuns, P. A. van Hal, S. A. Ponomarenko, H. G. Flesch, R. Resel, E. Cantatore, P. W. M. Blom, and D. M. de Leeuw, "Ordered semiconducting selfassembled monolayers on polymeric surfaces utilized in organic integrated circuits," *Nano Lett.*, vol. 10, no. 6, pp. 1998–2002, Jun. 2010.
- [21] K. Takahata, S. Aoki, and T. Sato, "Fine surface finishing method for 3dimensional micro structures," in *Proc. 9th IEEE Annu. Int. Workshop MEMS—Investigation of Micro Structures, Sensors, Actuators, Machines* and Systems, San Diego, CA, 1996, pp. 73–78.
- [22] F. K. Jiang, G. B. Lee, Y. C. Tai, and C. M. Ho, "A flexible micromachinebased shear-stress sensor array and its application to separation-point detection," *Sens. Actuators A, Phys.*, vol. 79, no. 3, pp. 194–203, Feb. 2000.
- [23] X. F. Zeng and H. R. Jiang, "Fabrication of complex structures on nonplanar surfaces through a transfer method," J. Microelectromech. Syst., vol. 20, no. 1, pp. 6–8, Feb. 2011.
- [24] X. F. Zeng, C.-C. Huang, and H. R. Jiang, "A transfer method for complex structures on fabricated on non-planar surfaces," in *Proc. 16th Int. TRANSDUCERS*, Jun. 5–9, 2011, pp. 402–405.
- [25] X. Feng, M. A. Meitl, A. M. Bowen, Y. Huang, R. G. Nuzzo, and J. A. Rogers, "Competing fracture in kinetically controlled transfer printing," *Langmuir*, vol. 23, no. 25, pp. 12555–12560, Dec. 2007.
- [26] D. H. Kim and J. A. Rogers, "Stretchable electronics: Materials strategies and devices," Adv. Mater., vol. 20, no. 24, pp. 4887–4892, Dec. 2008.
- [27] D. F. Zhu, C. H. Li, X. F. Zeng, and H. R. Jiang, "Tunable-focus microlens arrays on curved surfaces," *Appl. Phys. Lett.*, vol. 96, no. 8, pp. 081 111-1–081 111-3, Feb. 22, 2010.



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