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Fabrication of thick silicon dioxide sacrificial and isolation blocks in a silicon substrate

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Abstract
A silicon micromachining method that is able to create deep silicon dioxide blocks at selected locations in a silicon substrate is presented. The process combines deep-reactive-ion etching (DRIE), thermal oxidation, deposition of silicon dioxide and optional planarization. Design issues and parameters for the creation of such blocks are discussed. The selectively defined silicon dioxide blocks allow the integration of silicon surface and bulk micromachining and thick large-area isolation regions for integrated circuits. The performance enhancement that this approach enables is exemplified in the fabrication of an on-chip tunable capacitor and a monolithic transformer on 20-μm-deep silicon dioxide blocks.

1. Introduction

On-chip passive components have attracted a lot of interest in recent years because they are very important in radio-frequency (RF) circuits, which have widespread applications in wireless communication systems [1, 2]. The performance of current components, such as inductors, transformers and tunable capacitors, however, could be much improved. On-chip inductors and transformers generally suffer from low quality factors (Q) and low self-resonant frequencies (f_{res}) [1, 3–6]. One of the main reasons is the lack of a thick isolation layer between the device and the silicon substrate below. The eddy current induced in the substrate by the electromagnetic field generated by the inductor and the transformer introduces loss of energy and lowers Q [3, 5, 6]. Furthermore, the parasitic capacitance between the device and the substrates sets a limit to f_{res} of the device, thus its functional frequency range [4–6]. Current on-chip tunable capacitors, generally realized by electrostatically actuated parallel plates, have a similar problem. Because of the closeness between the bottom plate of the capacitor and the silicon substrate, the parasitic capacitance is on the same order of magnitude as the functional capacitance between the plates. Therefore, the tuning ratio of such capacitors is severely impaired [7]. A direct remedy to these issues is to deposit a thick layer of insulating material such as silicon dioxide [7]; the electromagnetic coupling and the parasitics between the devices and the substrate can be greatly reduced, thus enhancing the device performance. However, deposition of a very thick, say more than 10 μm, insulating film across the wafer, is hard to realize and will introduce other difficulties in processing such as making contacts with the substrate. The stress distribution in a thick deposited film can also induce a large bending moment on the substrate that would severely bend the wafer. The residual stress and built-in stress gradient of a thick deposited film may cause the film to crack as well. Other techniques have been developed to form 'localized' insulating layers in the substrate underneath specific devices, such as etching holes into the silicon substrate under particular devices and filling them with borophosphosilicate glass

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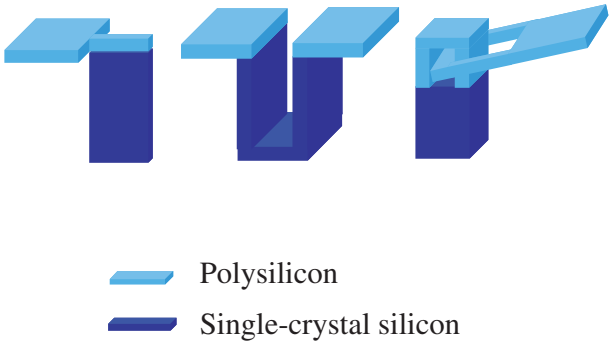


Figure 1. Schematic of the examples of fundamental mechanical structures that can be built by the integration of surface and bulk micromachining.

(BPSG) [8]. The improvements in the device performance, however, are typically limited. First, the thickness of the isolation layer is not significantly increased because refilling the deep and wide holes, if feasible at all, requires deposition of a thick film and produces large variation in topography. Second, silicon pillars still exist under the devices and are the sources of substrate loss previously discussed. An effective solution would be forming thick silicon oxide blocks, with relatively thin silicon oxide film, only beneath particular devices that require such isolation layers.

Silicon dioxide is widely employed as the sacrificial material in microelectromechanical system (MEMS) technologies, especially surface micromachining. For instance, multiple structural polysilicon and sacrificial silicon dioxide layers can be sequentially deposited and patterned to realize complicated and multilevel structures [9–11]. Despite the flexibility of surface micromachining, the intrinsic thinness of the deposited films can limit the performance of the device fabricated, such as electrostatic force produced by comb drives. On the other hand, deep-reactive-ion-etched (DRIE) structures boast large aspect ratio [12, 13] and excellent mechanical properties, as they use the single-crystal silicon. The combination of these two micromachining methods promises to keep the merits and overcome the limitations of each of them and to expand the design scope for silicon MEMS. For instance, figure 1 shows schematically some of the basic structures that can be realized by such integration. The challenge that arises is to create a flat surface for surface micromachining after the deep silicon structures are formed. A solution is to build the deep silicon structures amid silicon dioxide blocks that can be removed later.

In this paper, we describe in detail a MEMS process that can produce the desired thick silicon dioxide isolation and/or sacrificial blocks at designated areas in the silicon substrate [4, 14, 15], realized by sequential steps of etching deep narrow beam-and-trench structures in the silicon substrate with DRIE, thermal oxidation of the silicon beams, silicon dioxide deposition to seal the narrow openings left among the oxidized silicon beams and chemical mechanical polishing (CMP) to planarize the surface across the wafer. The depth of a silicon oxide block is mainly determined by the depth of the beam-and-trench structures etched; more than 20 μm in depth can be realized. Only a few micrometer thick silicon dioxide is employed in the creation of such a deep block, including the thermal oxide

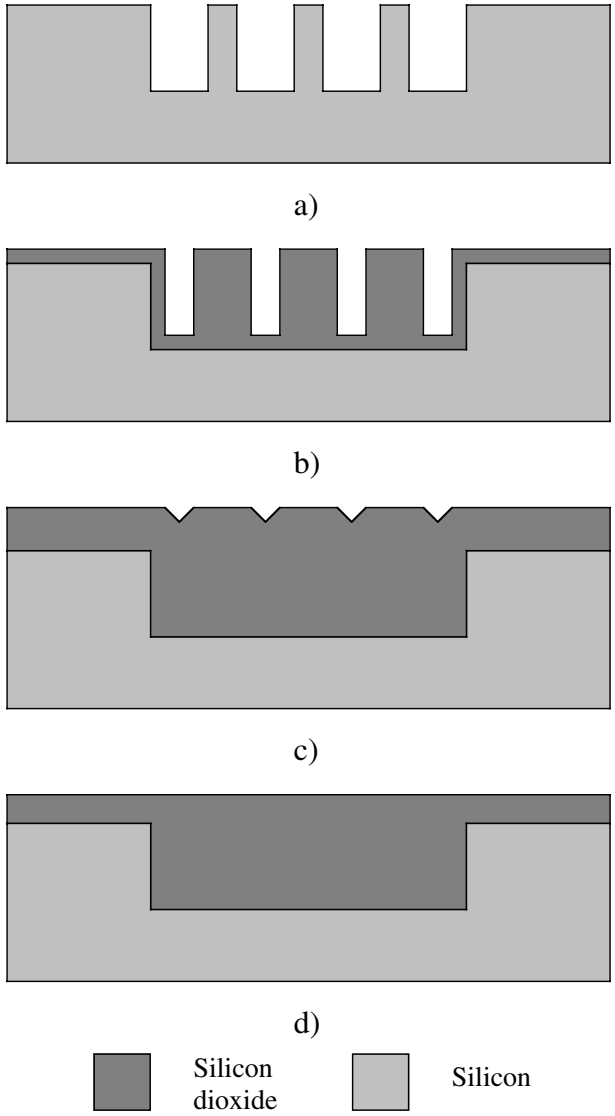


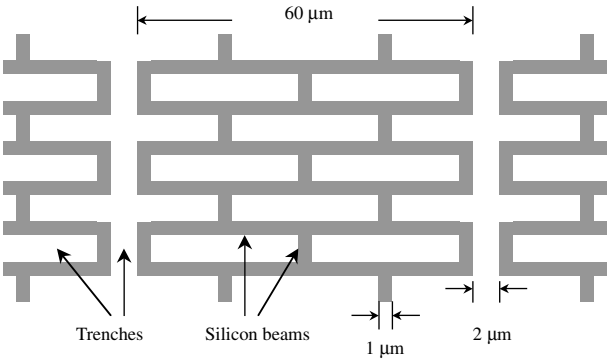
Figure 2. Schematic of the process flow that creates a silicon oxide block: (*a*) etching narrow beam-and-trench silicon structures by DRIE; (*b*) thermal oxidation of the beams; (*c*) sealing the gaps left after oxidation with silicon dioxide and (*d*) planarization of the surface.

transformed from the silicon beams and the deposited sealing oxide, no matter what the depth of the block is, because of the closely spaced beam-and-trench structures. Therefore, the problems caused by the stress in thick deposited silicon oxide films can be greatly reduced. The topography is smoother too, compared with refilling deep and wide holes or trenches.

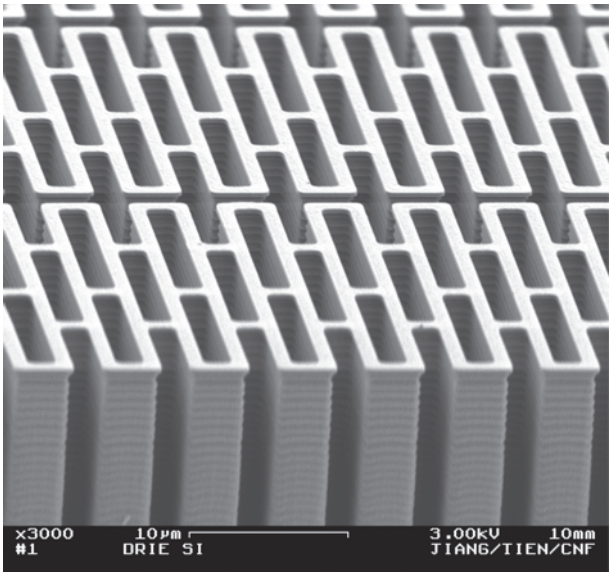
2. Process

2.1. Process concept

The challenge in the making of a thick silicon dioxide block discussed above rests in the creation of such a block at a specific area using relatively thin layers of silicon dioxide. Figure 2 gives a schematic of the process flow of our method to address these challenges. The whole procedures can be divided into the following steps:



(*a*)



(*b*)

Figure 3. (*a*) Schematic of the designed silicon beam-and-truss structures and (*b*) SEM image of such structures after DRIE. The depth of the etched silicon structures was 20 μm.

1. etching periodic deep beam-and-trench structures in the silicon substrate by DRIE (figure 2(*a*));
2. complete thermal oxidation of the silicon beams (figure 2(*b*));
3. deposition of silicon dioxide to seal the openings after the oxidation (figure 2(*c*));
4. optionally planarizing the surface of such a silicon dioxide block by CMP or etchback [16], so that later process steps can proceed from a flat surface (figure 2(*d*)).

In the first step, the area where the silicon dioxide block is to be placed is defined. Meanwhile, by etching those deep narrow beam-and-trench structures, the task of forming the silicon oxide block switches from growing thick silicon dioxide in the direction normal to the substrate to that growing silicon dioxide parallel to the substrate surface to form individual much thinner silicon dioxide blocks. Therefore, through the second and third steps, the block is formed with relatively thin silicon dioxide layers.

2.2. Process flow: an example

We use the formation of a 20-μm-deep, 400 μm $\times$ 400 μm silicon oxide block as an example to demonstrate the process flow. The design of such a process flow is deferred to the next section. The fabricated block would serve as the underlying insulation layer for the micromachined electrostatically actuated tunable capacitor and the monolithic transformer described in section 4. Processing was performed at the Cornell Nanofabrication Facility (CNF).

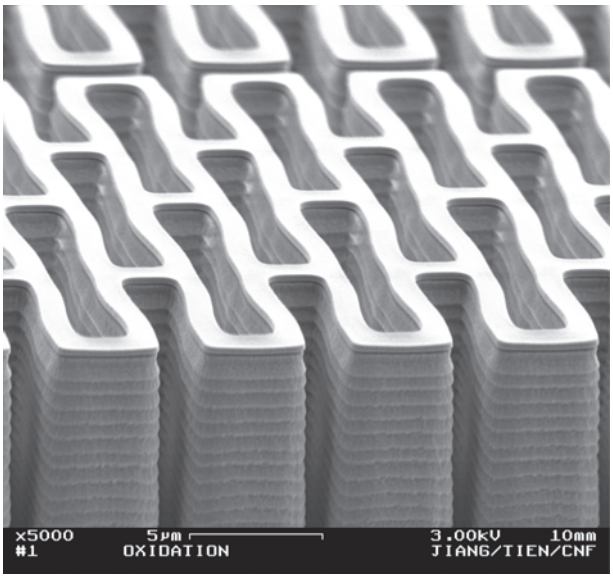


Figure 4. SEM image of the oxidized silicon beam-and-truss structures shown in figure 3. The maximum width of the gaps between adjacent oxidized beams was 2.5 μm.

First, we etched 20-μm-deep beam-and-truss structures in silicon substrate using DRIE. The width of the beams and trusses, w_b, was 1 μm; the spacing between adjacent beams, w_t, was 2 μm. Figure 3 shows the periodic beam-and-truss structure adopted, both the schematic plan view (figure 3(*a*)) and the SEM image (figure 3(*b*)). The DRIE was performed on a Plasma Therm SLR-770. Next, the DRIE structures were thoroughly wet oxidized for 260 min at 1100 °C (figure 4). A low-pressure chemical-vapor-deposited (LPCVD) silicon oxide 3 μm in thickness was then deposited, reacting with silane (SiH_4) and oxygen (O_2) at 425 °C. The openings left between the oxidized silicon DRIE structures were completely sealed after this step, as shown in the SEM image of the cross section of the formed silicon oxide block in figure 5. Finally, CMP was performed with Strasbaugh 6EC to form a flat silicon oxide surface (figure 6) onto which subsequent steps could be carried out.

3. Design issues

The process involves a few critical issues, including the widths of the beams and trenches, w_b and w_t, respectively, the design of the beam-and-trench structures and the type and thickness, t_{ox}, of the silicon dioxide film deposited to seal the openings after the oxidation of the silicon beams. These issues are closely related and depend heavily on the application and processing capability. Figure 7 shows schematically such dependence. Cost is another important factor. The most efficient way might not be the most economical one. An optimization of the fabrication process, therefore, could be

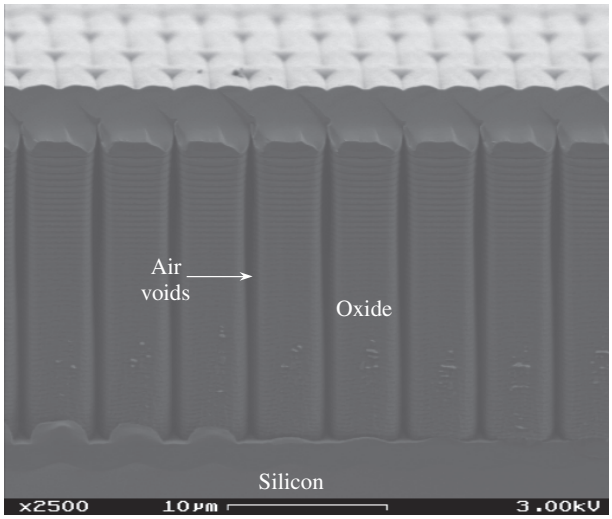


Figure 5. SEM image of the 20-μm-deep silicon oxide block formed after silicon oxide sealing. The deposited silicon oxide film was 3 μm in thickness and completely sealed the gaps between the oxidized beam-and-truss structures. Air voids in the block and ripples on the surface are clearly shown.

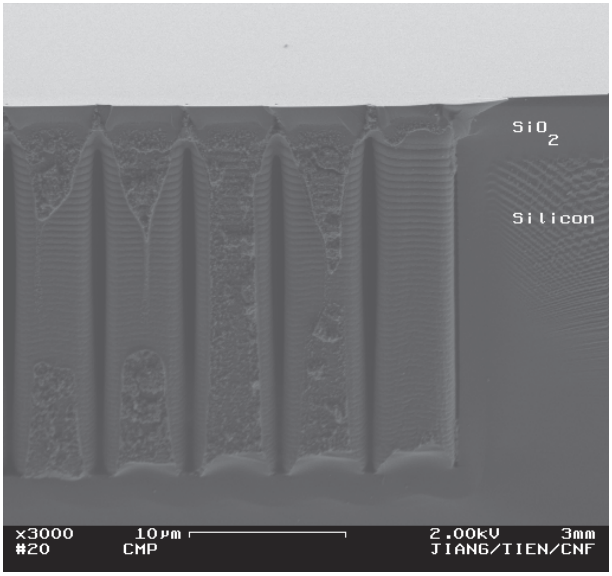


Figure 6. SEM of the 20-μm-deep silicon oxide block in figure 5 after CMP. The surface was completely planarized for later processing steps.

case-specific. In the rest of this section we will explain the guidelines to address these issues in detail.

3.1. Beam width

As already pointed out, the silicon beams serve as the 'skeleton' for the formation of the silicon oxide block after they are transformed to silicon dioxide through oxidation. Although there is no theoretical limit to the creation and oxidation of such beams, some practical factors do set the limit as to their width, w_b.

The first limiting factor is the time and the temperature allowed for the oxidation step. For instance, a long oxidation process at very high temperatures will lead to dopant diffusion

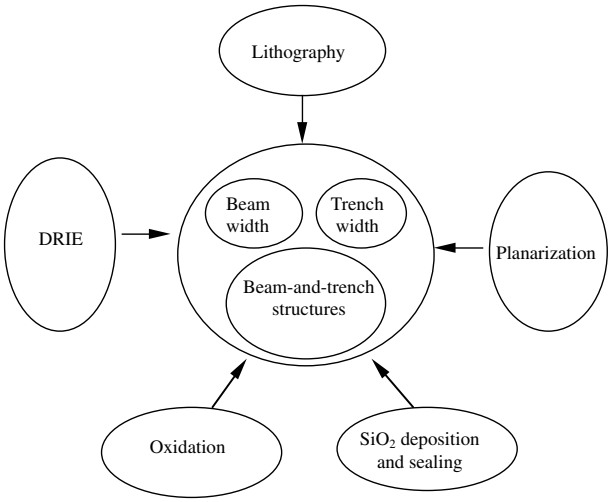


Figure 7. Factors that affect the design of the DRIE silicon structures.

in the wafer that might not be desired for some applications [16]. This means that the smaller w_b is, the better. If long oxidation at high temperature is allowed, however, the beams can be wider. On the other hand, the minimum line width that can be accomplished is limited by photolithography and DRIE capability.

Taking these two factors into account, we chose w_b as 1 μm, because line width as such can be produced by photolithography and etched through DRIE using Plasma Therm SLR-770, both in a reliable and reproducible manner, in CNF. For our devices, restriction in the oxidation time and temperature is not that stringent. The actual time and temperature of the oxidation process depend on the beam-and-trench structure as a whole and will be explained later.

3.2. Trench width

The high-aspect-ratio silicon beams are formed by etching periodical trench structures into silicon substrate via DRIE. Because in a later step, silicon dioxide is deposited to seal the gaps between the beams after oxidation, narrower trenches are preferred so that the sealing is easier.

The narrowness of these trenches, however, is first limited by DRIE. Too narrow a trench will make the etchant species very difficult to penetrate to the bottom of the trench, thus slowing down the etching process and creating a tapered profile of the beams—the bottom of the beam being wider than its top, which requires longer oxidation. Second, when the beam-and-truss DRIE structures, shown in figure 3, are adopted, the beams will buckle after oxidation, as explained later. If the trench is too narrow, two adjacent buckled beams will come into contact with each other, blocking oxidizing species to penetrate to the bottom of the trench, thus preventing further oxidation. In CNF, we have found that 1-μm-wide beams with 2-μm-wide trenches can be etched for 20 μm very reproducibly with a good profile (sidewall angles 90$\pm$1°). The beams shown in figure 3 can be thoroughly oxidized; the minimum spacing between adjacent beams after oxidation is 1.5 μm. Therefore we chose w_t as 2 μm.

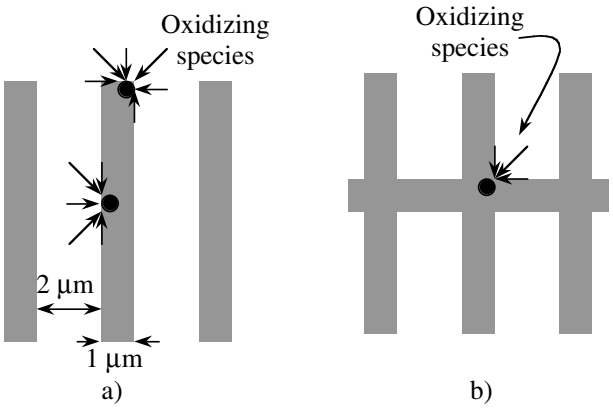


Figure 8. Diagram of the oxidation of simple silicon (*a*) beam and (*b*) grid structures; the width of the beams is 1 μm and that of the trenches is 2 μm. The arrows symbolize oxidizing species approaching from different angles. The inner corner of a grid in (*b*) is exposed to much less oxidizing species compared with any points in (*a*).

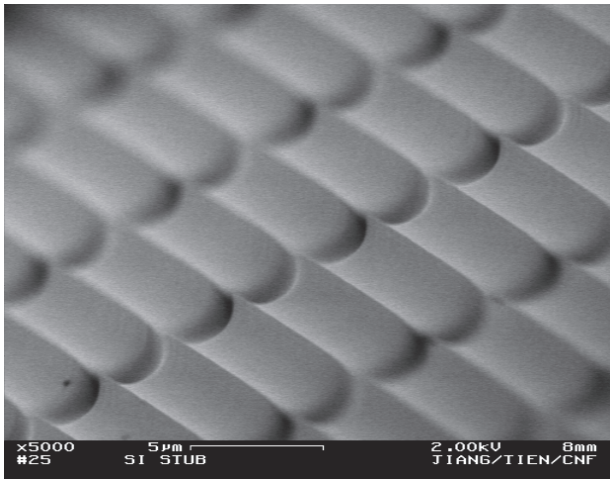
3.3. DRIE silicon structures

In this section we discuss the design of the DRIE silicon structures. Because the silicon structures need to be transformed into silicon oxide structures through oxidation, their design is affected by the oxidation condition. Another factor that needs to be considered is the mechanical strength of these silicon and silicon dioxide structures.

Unlike the oxidation of a planar silicon surface that is well described by the Deal–Grove model [16], the oxidation of high-aspect-ratio beam-and-trench structures is also affected by a phenomenon called *oxidation retardation* [17]. This is often believed due to a steric hindrance of the availability of the arriving oxidizing species and high stress in the structure, especially at the root of the beams [18, 19]. Therefore, to ensure oxidation of the silicon structures, longer oxidation may be required. To demonstrate this, we used two test structures, simple beams and grids, as shown in figure 8. The beam width is 1 μm, the trench width is 2 μm and the depth is 20 μm. Oxidation at 1100 °C was performed for 200 min, the time required to transform 0.5 μm of silicon into silicon dioxide for a planar silicon surface, and hydrofluoric (HF) acid was then applied to remove the silicon oxide. Figure 9 shows the SEM images of the residues left. While silicon stubs 1 μm high were left for the beams, silicon spikes with a height of 14 μm remained after the oxidation of the grid structures. As illustrated in figure 8, the inner corners of the grids are exposed to the least oxidizing species; therefore, they are expected to be more difficult and slower to oxidize. Another factor might be the higher stress at the joint points in the grid structures. Hence, grid structures should be avoided in the designed DRIE silicon structures, unless long exposure to the oxidation environment for better oxidation and/or the remaining silicon stubs is not a concern for a specific application.

The simple beam structures, however, have a weakness. It was observed that after oxidation of these beams and deposition of silicon oxide to seal the air gaps, the silicon oxide block thus created could not survive the CMP process. In most cases cracks occurred and in some cases part of the block peeled off. We believe that this is because our nonconformal silicon oxide deposition, discussed in the next section, can only *seal* the air gaps but cannot *fill* them (see figures 5 and 6). During the CMP process, the wafer is pressed and rotates against the polishing pad. The shear force thus exerted onto the transformed high-aspect-ratio silicon oxide beams might cause the crack and peeling. Nonetheless, the simple beam structures can be employed if other planarization methods, such as etchback, can be adopted, or if a conformal silicon oxide deposition as by decomposing tetraethoxysilane, $Si(OC_2H_5)_4$ or TEOS [17], is available to fill the air gaps completely.

Because we did not have access to a conformal silicon dioxide deposition and we needed the CMP planarization step for the manufacture of our devices, the final beam-and-trench structure we adopted was compromised, as already shown in figure 3. Lateral trusses 1 μm wide are introduced to join the 60-μm-long beams to enhance the resistance of the beams to the shear force during CMP. These trusses are offset to avoid a cross structure as shown in figure 8(*b*) to make the oxidation



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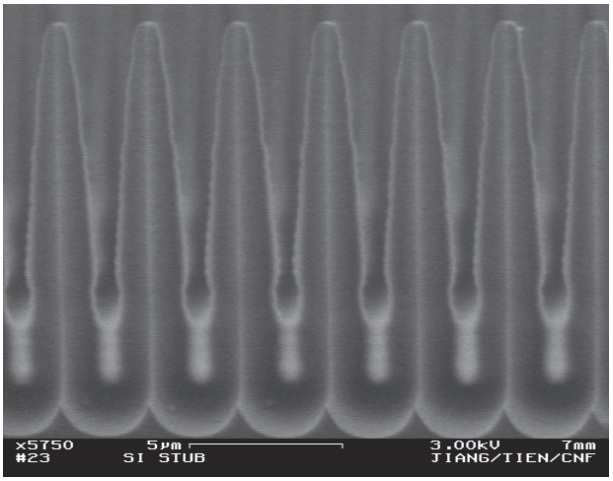

(*b*)

Figure 9. Silicon residue after oxidation and HF acid silicon dioxide removal for (*a*) simple beams and (*b*) grids. The height of the stubs is (*a*) 1 μm and (*b*) 14 μm, respectively.

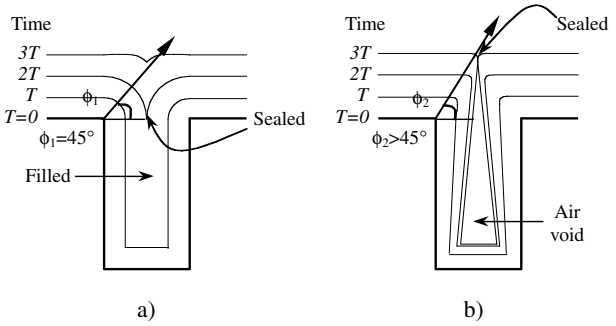

Figure 10. Schematic of the sealing of a trench by silicon oxide using (*a*) conformal and (*b*) nonconformal deposition as time evolves. The trench is completely filled with conformal deposition. The corners of the trench are moving upward at an angle of 45° because the deposition rates at the top surface and on the sidewalls are the same. With nonconformal deposition, the deposition rate at the top surface is larger than that on the sidewalls and the corners of the trench are moving upward at an angle larger than 45°. Thicker film is required to seal the trench than that required to fill the trench with conformal deposition; the sealing point is also higher. The trench cannot be filled but can only be sealed and an air void will be left after the sealing.

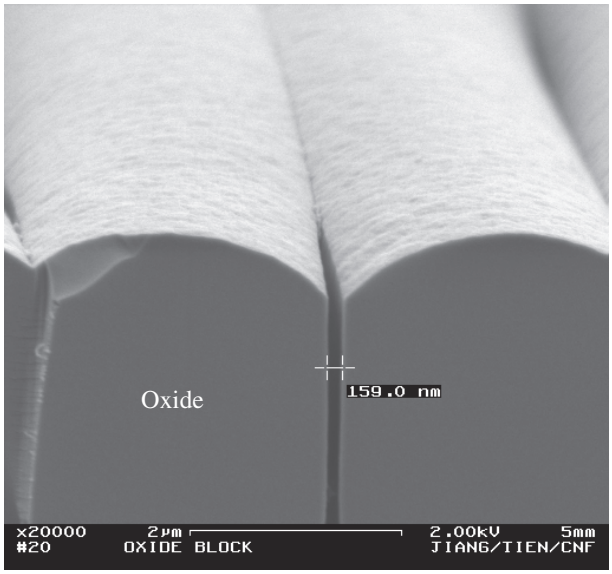

Figure 11. A 20 μm deep, 4 μm wide air gap barely sealed by 3.3 μm deposition of type B oxide; a gap 159 nm in width is still left.

retardation less severe. After oxidation, the volume of the beams expands by a factor of 2.27 [17]. The long beams and the trusses experience expansion in different directions, causing the beams to buckle and widening some of the air gaps. The widened air gaps make their sealing more difficult during the silicon oxide deposition, as discussed in the next section. Therefore, less buckling is preferred. The degree of buckling varies with the length of the beams. Generally speaking, the longer the beams are, the more the buckling, thus wider air gaps. On the other hand, structures with shorter beams with the trusses require a longer time for the pattern generator to make the mask for photolithography. The choice of 60-μm-long beams was what we found the best compromise between the maximum width of the air gaps and the amount of time required for pattern generation. In practice, the structures of beams and trusses underwent a wet oxidation of 260 min at 1100 °C, 1 h more than required to oxidize 0.5-μm-thick silicon for a planar silicon surface to better oxidize the joints of the beams and trusses. The observed maximum width of the air gaps after oxidation was 2.5 μm, much smaller than the upper limit of 4 μm we found, as will be explained next.

3.4. SiO_2 deposition

The purpose of silicon oxide deposition is to seal the air gaps left after the oxidation of the beams, thus, as mentioned above, creating much smaller individual blocks with relatively thin silicon oxide layer. Generally speaking, the lesser the need to seal the trenches is, the better. Therefore, better step coverage is more desirable.

Figure 10 schematically diagrams the trench sealing process with conformal and nonconformal deposited films. In the case of a conformal deposition, the deposition rate on the top surfaces is equal to that on the sidewalls of the trenches. Therefore, the corners of the trench moving upward at an angle of 45°. The trench is then sealed and completely *filled* after a deposition of half the width of the trench, regardless of its depth (figure 10(*a*)). On the other hand, when the deposition is nonconformal, the deposition rate on the top surfaces is higher than that on the sidewalls of the trench. Hence the corner growing upward at an angle larger than 45°. The sealing of the trench, therefore, requires more film deposition compared with the conformal case and air voids will be formed in the sealed trenches (figure 10(*b*)), also clearly shown in figures 5 and 6. These air voids, though, should not harm the performance of any device fabricated using this method. First, the silicon oxide layer will be removed later if it serves as a sacrificial layer. Second, for passive RF element application, a combination of air and silicon dioxide produces less parasitics than silicon dioxide alone since the permittivity of air is less than that of silicon dioxide. Another drawback of nonconformal deposition is that the trench sealing point is higher than the original top surface; the lesser the conformality of the deposition is, the larger this height difference. This means that later planarization cannot be performed all the way down to the original top surface; otherwise, the sealed trenches would be reopened. This might not be desirable for some applications.

In the fabrication of our devices, we required that the deposited silicon oxide be no thicker than 3 $\pm$ 0.3 μm, for the sake of later steps such as etching anchors in the silicon dioxide layer. In CNF, we have two options of LPCVD silicon dioxide, either using dichlorosilane ($SiCl_2H_2$) and nitrous oxide (N_2O) as the reactants at 900 °C (hereinafter described as type A oxide) or reacting silane (SiH_4) and oxygen at 425 °C (hereinafter described as type B oxide). Type A is more conformal than type B, resulting from the more rapid surface migration of the reactants or reactive intermediates at higher temperature growth conditions [17]. However, the deposition rate is only 3 nm min^{-1}, much slower than that of type B, which is 25 nm min^{-1}. Hence, we picked type B as our sealing silicon oxide. Up to 3.3 μm of type B oxide was deposited to seal air gaps of various widths. It was found that 4 μm was the threshold width of the air gaps to be sealed. Figure 11 is the SEM image of a 4-μm-wide gap that was barely sealed with 3.3 μm of type B oxide deposition. As explained in

the previous section, the maximum width of the air gaps after the oxidation of our beam-and-truss structures was 2.5 μm, smaller than the 4 μm limit. In practice we deposited 3 μm of type B oxide in order to get as thick an insulating film as possible and to leave more tolerance for the CMP step, which will thin down the silicon oxide layer.

4. Applications

In this section we demonstrate the applications of the process module to form thick silicon oxide blocks described above. In the first two examples, the block served as an underlying large-area isolation layer, while in the last two, it was a sacrificial block that enabled the integration of polysilicon surface- and single-crystal bulk micromachining.

4.1. A tunable capacitor

The first example is an on-chip tunable capacitor. It consists of two polysilicon plates, one fixed and one suspended by springs, separated by a silicon oxide sacrificial layer. The device is fabricated on a 20-μm-thick silicon dioxide block. The polysilicon plates will later be plated with copper after the removal of the sacrificial oxide for high conductivity [20]. When a voltage is applied between the two plates, the suspended plate will be attracted toward the fixed plate, thus changing the capacitance between the two plates. If the capacitor is built on a thick silicon oxide layer, the parasitic capacitances between the plates and the silicon substrate will be drastically diminished.

The fabrication started with growing and patterning a silicon nitride insulating layer, followed by the creation and planarization of a 20-μm-thick silicon oxide block onto which the device would be built. Next, two polysilicon layers were used to define the bottom plate and the top plate with suspension springs and etch holes. The first and second polysilicon layers were 2 and 1.6 μm in thickness, respectively, and were separated by a 1.8-μm-thick sacrificial silicon oxide layer, which would be etched away by HF acid later. The silicon oxide isolation block was only attacked at the periphery during this release step, since there were no etch holes in the bottom plate. Therefore, the bottom plate would stay fixed and attached to the silicon oxide block beneath. Finally, electroless copper plating was performed to coat copper onto the exposed polysilicon plates and springs to achieve low series resistance. Figure 12 shows the SEM image of a capacitor before HF acid release and copper plating (cross section) and after (bird's eye view in the inset of figure 12).

With the underlying 20 μm deep silicon dioxide isolation block, the parasitic capacitance between the bottom plate of the tunable capacitor and the silicon substrate would be reduced by a factor of 10, compared to that without such an isolation block, assuming an isolation layer of 2 μm thick silicon dioxide. Considering the air voids in the block, the parasitic capacitance is even further reduced in reality, because the permittivity of air is less than that of silicon dioxide. This reduction in the parasitic capacitances between the capacitor plates would improve the performance of the variable capacitor, such as the tuning ratio [7] and the resistance to substrate noise.

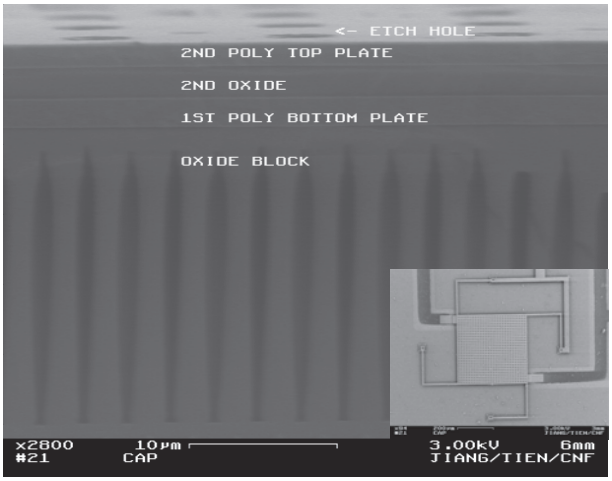

Figure 12. SEM picture of the cross section of a tunable capacitor before HF acid release and metallization and the bird's eye view of the device after (inset).

4.2. A monolithic transformer

In a recent study, we applied the 20-μm-deep silicon dioxide blocks to the fabrication of an on-chip transformer [21]. The isolation block greatly reduced the parasitic capacitance and electromagnetic coupling between the device and the lossy silicon substrate, thus increasing its Q and f_{res}.

The transformer structures, including the spirals and under/overpasses were fabricated on the blocks. They comprised two 1.4-μm-thick aluminum layers and a 1.4-μm-thick polyimide film in between as insulation. For comparison, the same transformer was fabricated nearby on chip without the underlying oxide block. The isolation layer between the first aluminum film and the silicon substrate was 4.1 μm of silicon oxide. Measurements showed that with the silicon oxide block, the maximum Q of the transformer was enhanced by over 100%, from 4.5 to 10.1; the f_{res} was increased by over 70% from 5.7 to 9.8 GHz.

4.3. Integration of surface and bulk micromachining

As mentioned in section 1, the silicon oxide sacrificial blocks can enable the integration of the surface and bulk micromachining. Our group has successfully demonstrated such integration.

In the first example [14], a 200 μm $\times$ 200 μm $\times$ 1.5 μm polysilicon membrane suspended by two polysilicon bars was driven by an electrostatic torsional actuator that consisted of two sets of comb drives at both ends—each composed of an array of fixed combs made of bulk silicon and another array protruded from the membrane and levitated above the fixed combs. This kind of membrane can potentially be utilized as a scanning micromirror in optical-fiber telecommunication systems.

The second example is a 1 mm $\times$ 2 mm $\times$ 1.2 μm biomimetic corrugated polysilicon diaphragm with attached single-crystal silicon proof masses [22]. With such proof masses, the first and second resonant frequencies of the diaphragm were reduced to 16 and 25 kHz, respectively.

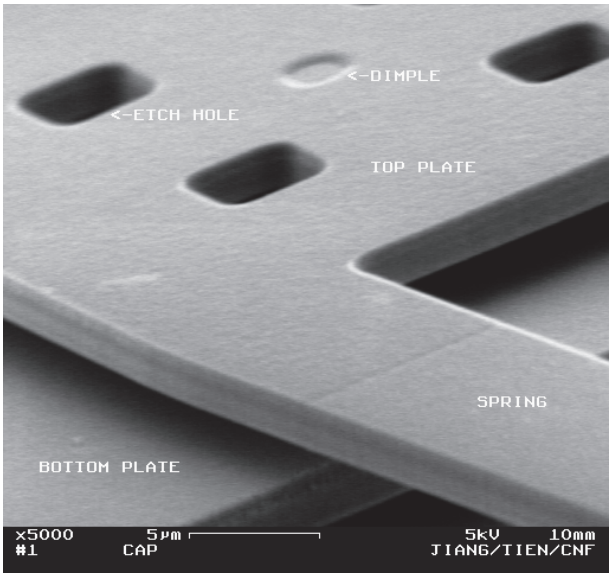

Figure 13. SEM image of a corner of the tunable capacitor with an underlying 20-μm-deep, 370 $\times$ 370 μm^2-large silicon oxide block (not shown). The top polysilicon plate is suspended by springs anchored to the edges of the block. The flatness of the top plate and the spring suggests that there is no apparent detrimental effect of the isolation block on the device structures.

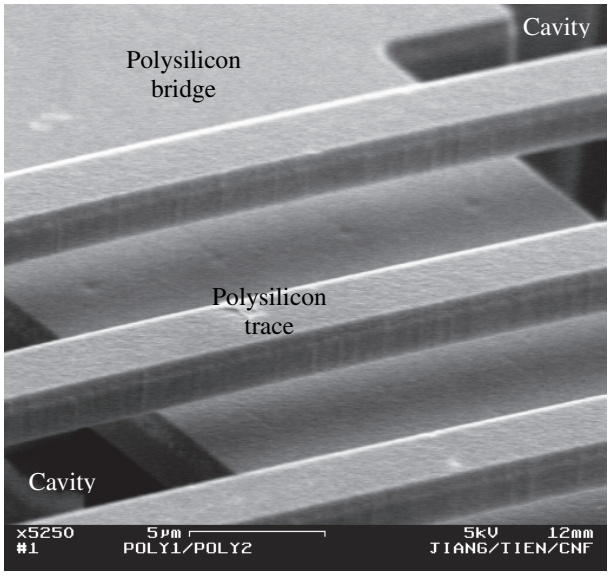

Figure 14. SEM image of a part of a polysilicon spiral suspended by two polysilicon bridges (only one shown) anchored to the edges of the cavity, formed after the removal of the underlying 20-μm-deep, 400 $\times$ 400 μm^2-large sacrificial silicon oxide block. Each trace of the spiral is 2 μm thick, 4 μm wide and at least 100 μm long. No distortion of the bridges and the spiral was observed. This suggests that the silicon oxide block does not affect the device structures as a sacrificial layer either.

Frequencies between these two resulted in the linear combination of the two modes, producing an asymmetric shape of the diaphragm corresponding to the direction of the acoustic source. The diaphragm can be applied to the fabrication of directional hearing aids.

5. Discussion

Our approach to form localized thick silicon oxide blocks only utilizes a few micrometer thick silicon oxide. The problems caused by the deposition of thick films, such as the warping of the substrate and cracking of the film due to stress distribution, built-in stress gradient and residual stress, are reduced. Furthermore, the air voids in the silicon oxide blocks might help relieve the stress. It is worthwhile to study whether the silicon oxide blocks, either as isolation or as sacrificial layers, have any negative effects on the structures and the functions of the devices built onto them. Figure 13 shows the SEM image of a corner of the tunable capacitor with an underlying 20-μm-deep, 400 $\times$ 400 μm^2-large silicon oxide block. The top polysilicon plate is suspended by springs anchored to the edges of the block. The flatness of the top plate and the spring suggests that there is no apparent detrimental effect of the isolation block on the device structures. Figure 14 shows a close-up of a polysilicon spiral suspended by two polysilicon bridges (only one is shown) anchored to the edges of the cavity, formed after the removal of the underlying 20-μm-deep, 400 $\times$ 400 μm^2-large sacrificial silicon oxide block. Each trace of the spiral is 2-μm thick, 4-μm wide and at least 100-μm long. No distortion of the bridges and the spiral was observed. This suggests that the silicon oxide block does not affect the device structures as a sacrificial layer either.

6. Conclusion

We have developed a process module through which silicon dioxide sacrificial and/or isolation blocks can be created in the silicon substrate. The formation of such a silicon oxide block consists of the patterning of narrow beam-and-trench silicon structures by DRIE, thorough thermal oxidation of these structures, silicon oxide deposition to seal the gaps between the oxidized beams and an optional CMP step to planarize the silicon dioxide surface. The actual construction of the process flow, such as the design of the high-aspect-ratio silicon structures, choice of oxidation time and condition, choice of type and thickness of silicon oxide deposited to seal the air gaps after oxidation, depends on the application and the facility capability. Design issues for the creation of such blocks are discussed. The silicon dioxide blocks fabricated at designated areas in silicon substrate allow the integration of silicon surface and bulk micromachining and thick large-area isolation regions for integrated circuits. The performance enhancement this approach enables is exemplified in the fabrication of an on-chip tunable capacitor and a monolithic transformer on 20-μm-deep silicon dioxide blocks.

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