# On-Chip Spiral Inductors Suspended over Deep Copper-Lined Cavities

Hongrui Jiang, Ye Wang, Jer-Liang Andrew Yeh, and Norman C. Tien

***Abstract*—A silicon micromachining method has been developed to fabricate on-chip high-performance suspended spiral inductors. The spiral structure of an inductor was formed with polysilicon and was suspended over a 30-$\mu$m-deep cavity in the silicon substrate beneath. Copper (Cu) was electrolessly plated onto the polysilicon spiral to achieve low resistance. The Cu plating process also metallized the inner surfaces of the cavity, forming both a good radio-frequency (RF) ground and an electromagnetic shield. High quality factors ($Q$s) over 30 and self-resonant frequencies higher than 10 GHz have been achieved. Study of the mechanical properties of the suspended inductors indicates that they can withstand large shock and vibration. Simulation predicts a reduction of an order of magnitude in the mutual inductance of two adjacent inductors with the 30-$\mu$m-deep Cu-lined cavity from that with silicon as the substrate. This indicates very small crosstalk between the inductors due to the shielding effect of the cavities.**

***Index Terms*—Electroless copper plating, electromagnetic shielding, integration of surface and bulk micromachining, microelectrical mechanical system (MEMS), on-chip inductor, $Q$ factor, radio-frequency (RF) device, silicon micromachining, suspended coil.**

## I. Introduction

ON-CHIP inductors are valuable components in radio-frequency (RF) circuits, which have widespread applications in wireless communication systems [1]–[3]. Current on-chip inductors typically have low quality factors ($Q$s), lack good RF grounds, have characteristics dependent on the substrate geometry [4] and electromagnetic coupling with the surrounding ambient, and have low self-resonant frequencies ($f_{\rm res}$) [5]. Many techniques have been developed to reduce the substrate loss and/or parasitics due to the substrate, such as using a high-resistivity silicon substrate [1], [6], silicon on sapphire [7], [8], silicon on glass [9] or quartz [10], etching away the silicon substrate under the device [11], [12], and building the inductor on a thick silicon-oxide layer [5]. Among these methods, removing the silicon substrate beneath the inductor minimizes the substrate loss and parasitic capacitance. However, the mechanical robustness of the inductor structure is a concern and additional fabrication steps, such as bonding a low-loss superstrate to the circuit area, may be required to improve the mechanical robustness [11]. Metal ground lines are placed around the inductors in these methods, which consumes more device area. In addition, these approaches do not diminish the electric and magnetic coupling among the devices, which might introduce large crosstalk. A patterned metal shield can be inserted beneath the inductor to provide an electromagnetic shield and to reduce the crosstalk [4], [13], but the benefit is counteracted by the loss induced within the inserted shield itself.

We address the issues described above concurrently by building a suspended inductor over a cavity whose bottom plane and sidewalls are metallized with copper (Cu) [14]–[16]. The deep cavity substantially reduces the electromagnetic coupling and the parasitic capacitance between the inductor and the silicon substrate, thus increasing $Q$ and $f_{\rm res}$. The polysilicon spiral inductor is electrolessly plated with Cu for small series resistance. The same plating process coats the silicon bottom plane and sidewalls of the cavity with Cu as well, providing both a good RF ground and an electromagnetic shield that isolates the device from its environment. Provided that the cavity is deep enough, the eddy current induced in this metal shield by the magnetic field generated in the inductor will be small, and so will be the resulting power loss. The Cu-lined cavity does provide electromagnetic shielding. The electromagnetic field generated by the inductor cannot penetrate deep into the Cu surface because of the exponential decay that the electromagnetic waves undergo when propagating into a conductor. The depth of such penetration can be described by the skin depth, which will be discussed in length in later sections. For RF frequencies higher than 1 GHz, the skin depth is on the order of 1 $\mu$m. Therefore, the electromagnetic field is practically confined within the cavity, and the coupling to the ambient is very small. Metal routing is also easily realized by exposing silicon and polysilicon wiring for Cu deposition. Fig. 1 shows the schematic of the cross section of a Cu encapsulated inductor. Polysilicon is chosen as the structural material for two reasons. First, polysilicon is a stiff material [17] that can better withstand environmental shocks and vibrations. Second, polysilicon surface micromachining is well established and has the flexibility to construct complex structures [18].

## II. Fabrication

The inductors described above were fabricated at the Cornell Nanofabrication Facility (CNF). Fig. 2 shows the scanning electron micrograph (SEM) image of a typical rectangular inductor. A schematic of the process flow is given in Fig. 3. The whole fabrication procedures can be divided into three major phases:

1) creation of the sacrificial silicon-oxide blocks in the areas where the cavities are to be defined;

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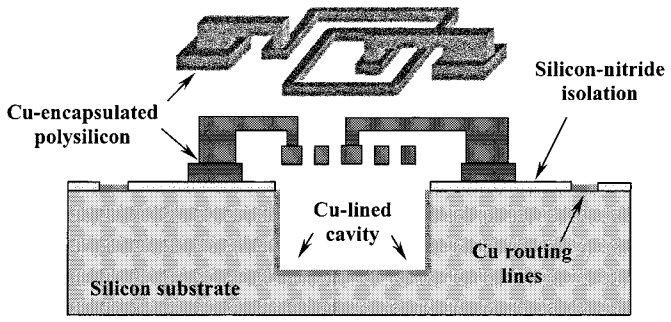


Fig. 1. Schematic of a copper-encapsulated polysilicon inductor suspended over a copper-lined cavity beneath.

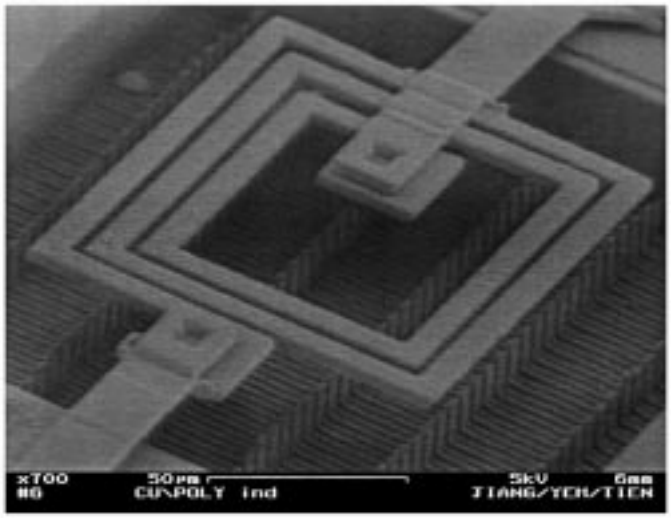

Fig. 2. SEM image of a suspended rectangular spiral inductor.

2) construction of the inductor structures through two-layer polysilicon surface micromachining;
3) electroless Cu plating for the purpose of metallization.

The processing details are related below.

### A. Creation of $SiO_2$ Blocks

In the areas of the deep cavities beneath the inductors, sacrificial silicon-oxide blocks were first formed, onto which the device structures were constructed. The approach to the formation of such blocks was etching deep narrow beam-and-trench structures out of bulk silicon and subsequently transforming such silicon structures to silicon oxide.

First, a 650-nm-thick low-pressure chemical-vapor-deposited (LPCVD) silicon-nitride film was grown on the silicon substrate at the temperature of 850 °C [Fig. 3(a)]. This film served as the isolation layer. The areas where the sacrificial silicon-oxide blocks were to be defined were then opened by removing this silicon-nitride isolation layer through fluorine-based reactive ion etch (RIE). The patterns of the first metal routing lines were formed as well in this step by etching away the silicon nitride and exposing the silicon substrate.

The 30-$\mu$m-deep sacrificial silicon-oxide blocks were then created. First, we etched 30-$\mu$m-deep beam-and-trench structures using deep reactive ion etch (DRIE) [Fig. 3(b)]. The widths of the beams and the trenches were 1 and 2 $\mu$m, respectively.

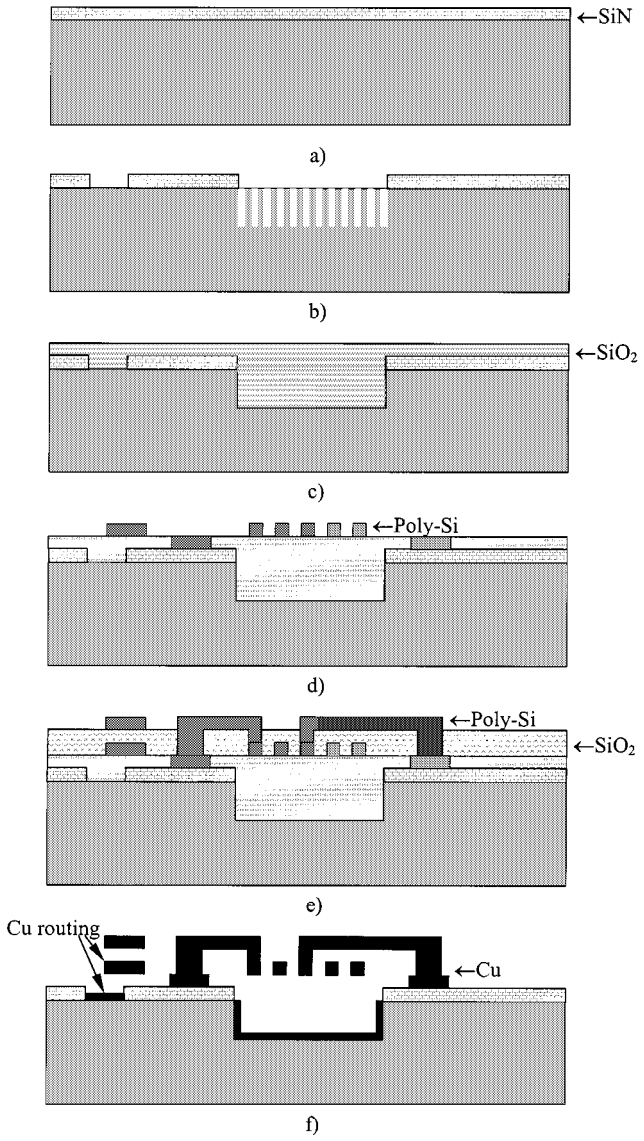


Fig. 3. Schematic of the fabrication process flow: (a) deposition and patterning of isolation silicon nitride; (b) etching narrow beam-and-trench structures for the sacrificial silicon-oxide block by DRIE; (c) thermal oxidation, silicon-oxide deposition, and CMP to form the sacrificial block; (d) deposition and patterning of the first polysilicon structural layer; (e) deposition and patterning of the second sacrificial silicon-oxide and polysilicon structural layers; and (f) RTA, HF release, and electroless Cu plating.

Thorough thermal oxidization of the silicon beams at 1150 °C was then performed for 5 h. Afterwards, a 3-$\mu$m-thick LPCVD silicon oxide was deposited at 900 °C to completely seal the openings left after thermal oxidation. LPCVD silicon oxide was chosen because of its high conformality. The SEM image of the cross section of a silicon-oxide block thus formed is shown in Fig. 4. Ripples on the surface after the sealing of the openings by silicon oxide are clearly shown. In the blocks there existed some air gaps owing to the bending of the oxidized beams. These air gaps affected neither the following processing procedures nor the performance of the inductors after the removal of the sacrificial silicon oxide. Next, chemical mechanical polishing (CMP) was performed to planarize the silicon-oxide surface [Fig. 3(c)]. This silicon-oxide film also acted as the first sacrificial layer in the surface micromachining process described below.

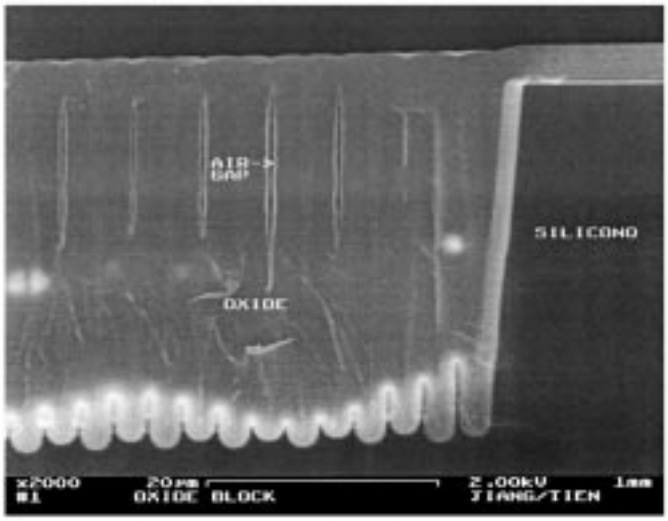


Fig. 4. SEM image of the cross section of a 30-$\mu$m-deep sacrificial silicon-oxide block.

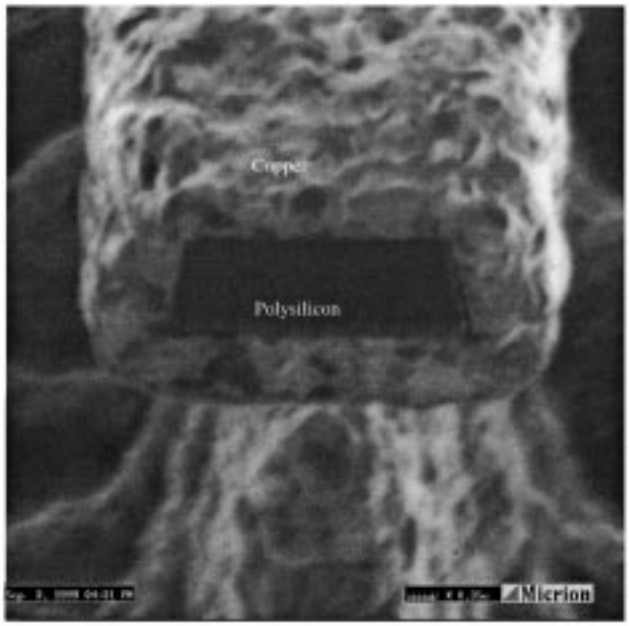


Fig. 5. Focus ion beam micrograph of the cross section of a copper-encapsulated polysilicon strip.

### *B. Construction of the Inductor Structures*

We produced the inductor structures [Fig. 3(d) and (e)] through a conventional two-layer polysilicon surface micromachining process, where two polysilicon layers served as the structural materials.

A photolithography step was first used to pattern and etch anchor openings, through which the inductor structures were fixed onto the silicon-nitride isolation layer. The first 1.5-$\mu$m-thick p-type LPCVD polysilicon film was then deposited at 620 °C, *in situ* doped with diborane ($B_2H_6$) as the boron source. An LPCVD silicon-oxide layer with the thickness of 250 nm was deposited, patterned, and utilized as hard masks for etching this polysilicon layer underneath. Thermal annealing at the temperature of 1000 °C for about 1 h was performed after the deposition of this masking silicon-oxide to release the interfacial stresses between different deposited films. Then the first polysilicon layer was etched, by chlorine-based RIE, to form the spirals and the second-level metal wiring.

Next, a second 3-$\mu$m-thick LPCVD silicon-oxide film was deposited as the second sacrificial layer, followed by a photolithography step to pattern vias. Then the second polysilicon structural film was deposited and patterned, in the same way described above, to construct the third-level metal wiring and the overpasses, which connected the input and output ports across the spiral traces and the cavity edges to probing pads on the verges of the cavities. The manufacture of the inductor structures concluded with a rapid thermal annealing (RTA) step at the temperature of 1100 °C for 90 s to minimize the stress gradient.

### *C. Electroless Cu Plating*

The final phase in the fabrication of the inductors was electroless Cu plating. This is a low-temperature process (55–80 °C) that introduces little thermal stress and is compatible with IC techniques as a postprocess procedure.

The plating procedures started with a wet activation step, where the silicon and polysilicon surfaces were stripped of the native silicon oxide by hydrofluoric (HF) acid and a catalytic palladium (Pd) activation film was formed onto them. This Pd activation film served as the base metal for Cu deposition later. Silicon nitride surfaces, on the other hand, were not activated during this step; therefore, they would remain inactive to Cu deposition and would provide isolation. The devices were finally dipped in a base solution that contained cupric sulphate and formaldehyde as the reduction agent. The following reaction occured [15]:

$$Cu^{2+} + 2HCHO + 4OH^{-} = Cu + H_2 + 2H_2O + 2HCOO^{-}.$$

The structures were first released in HF to remove the sacrificial silicon oxide, followed by electroless Cu deposition described above [Fig. 3(f)]. The exposed silicon and polysilicon structures, including the routing lines, spiral inductors, overpasses, and inner surfaces of the cavity beneath, were plated with Cu. Saturation was observed after long depositions over 30 min. For 15 min of plating at 60 °C, the thickness of the Cu deposited onto spiral strips was 0.75 $\mu$m. A self-assembled monolayer (SAM) of octadecyltrichlorosilane ($C^{18}$ OTS) was deposited onto the Cu structures to protect them from corrosion [19]. The resistivity $\rho$ of the plated Cu was measured to be 2.1 $\mu\Omega$-cm. Fig. 5 is the focus-ion-beam (FIB) image of the cross section of a polysilicon coil fully encapsulated with Cu. As is clearly demonstrated, the plating was conformal.

## III. Design Aspects

A complete inductor consists of the polysilicon spiral, overpasses, the cavity beneath and the copper electrolessly plated onto the spiral, overpasses, and the inner surfaces of the cavity (Fig. 6). The rectangular shape of the spiral was adopted for the inductors because of the convenience in simulation using finite-element method (FEM). Physical parameters that are used to describe a rectangular inductor include:

$n$ number of turns of the spiral;
$t_s$ thickness of the polysilicon strip;

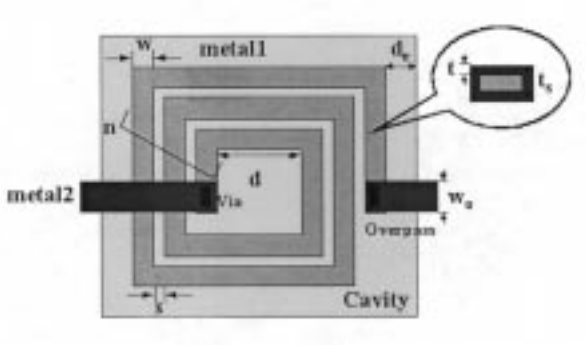


Fig. 6. Schematic of the plan view of a rectangular spiral inductor.

TABLE I
VALUES OF THE PARAMETERS OF THE INDUCTORS DESIGNED AND FABRICATED

| Parameters | *Ind1* | *Ind2* | *Ind3* |
|---|---|---|---|
| $n$ | 3 | 5 | 7 |
| $w$ (μm) | 3 | 5 | 6 |
| $s$ (μm) | 3 | 3 | 4 |
| $d$ (μm) | 125 | 75 | 125 |
| $t_s$ (μm) | 1.5 | | |
| $w_o$ (μm) | 18 | | |
| $d_c$ (μm) | 30 | | |
| $t$ (μm) | 0.75 | | |
| $d_e$ (μm) | 30 | | |
| $L\|_{1\text{GHz}}$ (nH) | 1.8 | 2.7 | 8.2 |
| $C_p$ (fF) | 13.1 | 16.0 | 28.9 |
| $R_s\|_{1\text{GHz}}$ (Ω) | 2.7 | 3.7 | 8.4 |

$d$ length of the innermost polysilicon strip of the spiral;
$s$ spacing between adjacent parallel polysilicon strips,
$w$ width of the polysilicon strip;
$t$ thickness of the copper deposited;
$d_c$ depth of the cavity;
$d_e$ closest distance between the spiral and the edge of the cavity;
$w_o$ width of the overpasses.

The values of the parameters of the three inductors designed and fabricated, labeled *Ind1*, *Ind2*, and *Ind3*, are listed in Table I. In this section, we explain in detail how these parameters were determined. An FEM simulator, Microcosm MEMCAD [20], was utilized extensively to this end.

### A. Design of the Spiral

For most applications in wireless communications, the required inductance is around a few nanohenries. To reach this inductance range, three to seven turns in the spiral were needed. The thickness of the polysilicon films $t_s$ was chosen to be 1.5 $\mu$m, which is common in polysilicon surface micromachining. The length of the innermost polysilicon strip $d$ was chosen to be 75 or 125 $\mu$m. The area occupied by a spiral ranged from 150 $\times$ 150 $\mu$m$^2$ to 250 $\times$ 250 $\mu$m$^2$. Large $d$ was used because the innermost turns of the spiral would have enormous resistance, owing to the eddy current generated in them at high frequencies, and their contributions to the inductance would be small as well [21]. For the same reason, vias between the first and second polysilicon layer were offset from the center of the spiral so that the overpasses could avoid the strong magnetic field in the central region of the spiral.

The spacing between two adjacent parallel strips $s$ was set to be 3 or 4 $\mu$m based on two factors. First, the smaller $s$ is, the larger the magnetic coupling between the strips, and thus the larger inductance given the layout area, while the interwinding capacitance between the strips is reported to have negligible effect upon the inductor performance [22]. Second, variation in the fabrication process and mechanical shock and vibration from the environment, as discussed later, demand a certain spacing tolerance. Taking these two factors into account, nominal $s$ of 3 or 4 $\mu$m was adopted. After the conformal Cu plating, the effective $s$ would drop to 2 or 3 $\mu$m.

The width $w$ of the polysilicon strips is another important parameter of an inductor. In general, wider strips have smaller series resistance $R_s$. However, larger $w$ inevitably causes larger device area and parasitic capacitance to the substrate. Furthermore, simulation by Craninckx *et al.* [21] shows that too wide a strip can produce very large resistance, due to skin effect, at high frequencies. Consequently, we opted for relatively narrow strip widths. The actual width of the inductor strip was increased by about 1.5 $\mu$m, twice the thickness of the plated Cu, after Cu plating.

### B. Thickness of Plated Cu

Low series resistance $R_s$ of the inductor, including two overpasses, was achieved by plating the polysilicon spiral with Cu. We simulated $R_s$ with varied Cu thickness $t$. The results for *Ind2* are shown in Fig. 7(a) as an example. The effective $t$ was more than doubled because Cu was deposited onto all sides of the polysilicon strip. The following discussion applies to the other two inductors as well, although data are not shown. Observing Fig. 7(a), we can conclude that the thicker the deposited Cu is, the smaller $R_s$ is. However, $R_s$ is not reduced linearly with $t$, especially at frequencies higher than 10 GHz, where dramatic increase in $R_s$ is observed from Fig. 7(a). This phenomenon is again due to the skin effect. The skin depth can be calculated by

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}} = \frac{2.3}{\sqrt{f}}\ \mu\text{m}$$

where $\rho$ is the resistivity of the plated Cu, measured to be 2.1 $\mu\Omega$-cm; $\mu$ is the permeability, equal to $4\pi \times 10^{-7}$ H/m; and $f$ is the frequency in gigahertz. For a frequency range from 1 to 10 GHz, which is of most interest in wireless communication, $\delta$ varies from 0.7 to 2.3 $\mu$m. Hence, $t$ of 2 $\mu$m should be reasonable. However, as discussed in the previous section, only a thickness of 0.75 $\mu$m was reached during the Cu plating. The achievement of thicker deposited Cu is the goal of future work.

Simulation results of the inductance $L$ of *Ind2* with different $t$ and $f$ are shown in Fig. 7(b). As can be seen, $L$ shows slight variation around 10% and is not very sensitive to either $t$ or $f$. The insensitivity of $L$ to $f$ is consistent with the results reported by Yue *et al.* [13].

### C. Design of the Cavity

The deep Cu-lined cavity beneath the inductor provides electromagnetic shielding and small parasitic capacitance. On the

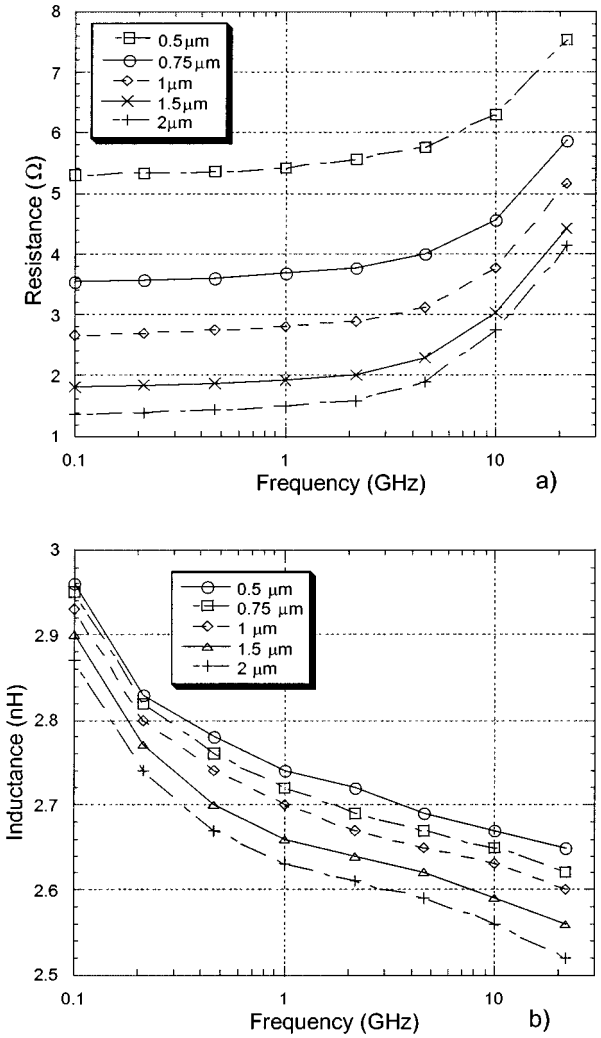


Fig. 7. Simulated (a) $R_s$ and (b) $L$ of *Ind2* with varied thickness of plated copper.

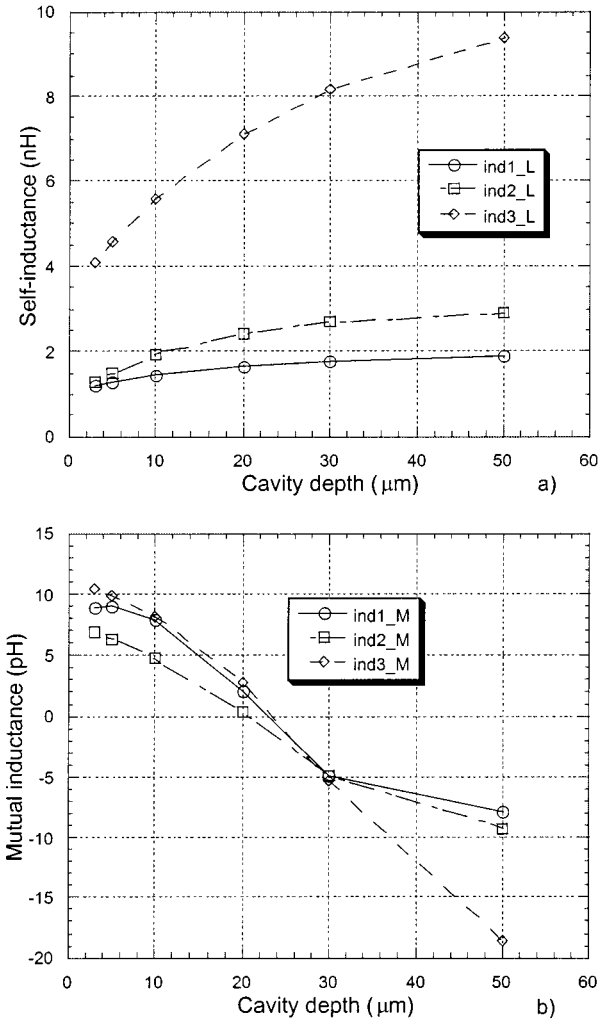


Fig. 8. Simulated (a) self- and (b) mutual inductances of pairs of identical inductors versus the cavity depth.

other hand, the level of difficulty in the creation of such a cavity rises as the depth increases. Therefore, a compromise must be made, and a reasonable cavity depth $d_c$ was found.

To investigate the shielding effect quantitatively, we studied the mutual inductances between and self-inductances of pairs of identical inductors juxtaposed 25 $\mu$m apart at the frequency of 1 GHz. Fig. 8 gives the simulation results with varied $d_c$. A couple of observations are noteworthy. First, the self-inductance $L$ increases as $d_c$ increases. To understand this phenomenon, it may be convenient to introduce the concept of virtual image currents of the original one flowing in the spiral with respect to the Cu cavity surfaces, similar to that well known in electrostatics. These image currents, along with eddy currents induced in the shield, produce their own magnetic fields opposite to the one generated by the original spiral. Hence, the total magnetic field is reduced and the inductance is decreased from the nominal inductance of the spiral itself. As $d_c$ increases, this reduction is less severe because the distance between the original spiral and the image and eddy currents increases; thus there is less coupling in between. As shown in Fig. 8(a), when $d_c$ is around 30 $\mu$m, $L$ levels off for all three of the inductors. The virtual attribute of these image currents should be stressed, however, because they merely provide a handy way of understanding the redistribution of magnetic field owing to the Cu shield. Unlike real currents such as eddy currents, these virtual image currents do not incur power dissipation.

The second interesting phenomenon is that mutual inductance $M$ between two adjacent identical inductors changes not only in value but in sign as well [Fig. 8(b)]. To better understand this, we simulated $M$ using different types of substrate, including air (equivalent to not having any substrate at all), silicon (resistivity 3 $\Omega$-cm), and Cu, all positioned 2 $\mu$m under the inductors, compared with 30-$\mu$m-deep Cu-lined cavities beneath the inductors. The results are outlined in Table II. When the two inductors are suspended in the air, $M$ stems solely from the magnetic coupling between the two spirals. When a substrate is under the spirals, image and eddy currents in the substrate also contribute to the magnetic coupling to the other spiral. This effect, while very weak in the case of silicon, is most conspicuous with Cu substrate, where the combined effect changes the sign of $M$ and dramatically reduces its absolute value. As $d_c$ increases, the effect of the image current becomes less significant because it be-

TABLE II
MUTUAL INDUCTANCES OF PAIRS OF IDENTICAL INDUCTORS WITH DIFFERENT SUBSTRATES BENEATH

| $M$ (pH) | Air | Silicon substrate | Cu substrate | Cu cavity |
|---|---|---|---|---|
| *Ind1* | -22.7 | -22.6 | 9.4 | -4.9 |
| *Ind2* | -27.2 | -25.3 | 6.7 | -4.9 |
| *Ind3* | -110.2 | -108.0 | 12.9 | -5.3 |

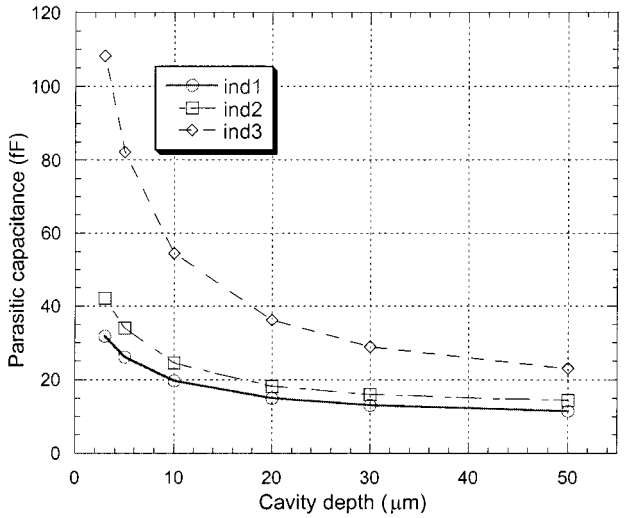


Fig. 9. Simulated parasitic capacitances of the inductors versus the cavity depth.

comes weaker. At a certain depth, around 20–30 $\mu$m, as indicated in Fig. 8(b), $M$ drops to zero as the contributions from the spiral, image, and eddy currents cancel out. As $d_c$ increases further, the contribution from the spiral becomes more and more dominant and $M$ changes sign again, back to the case of an "air" substrate. The explanation above is qualitative, and further, extensive simulation is needed for the full understanding of this phenomenon.

Summarizing the results given in Fig. 8, we chose $d_c$ to be 30 $\mu$m. As shown in Table II, with the Cu-lined cavity, $M$ is reduced tremendously compared with "air" or silicon substrate, by almost a factor of 20, in the case of *Ind3* to a few picohenries, and is two to three orders of magnitude smaller than the self-inductances. Therefore, the magnetic coupling between inductors is expected to be extremely small.

Fig. 9 gives the parasitic capacitances $C_p$ with $d_c$ varying from 3 to 50 $\mu$m for all three inductors. At 30 $\mu$m, $C_p$ is already decreased significantly, and not much improvement can be accomplished by increasing $d_c$ further. The self-resonant frequency $f_{\rm res}$ of an inductor can then be estimated by

$$f_{\rm res} \approx \frac{1}{2\pi\sqrt{LC_p}}.$$

Assuming $C_p \approx 30$ fF and $L \approx 5$ nH, we have $f_{\rm res} \approx 10$ GHz, indicating a wide functional frequency range of the inductors. Finally, the closest distance between the spiral and the cavity edges $d_e$ was prescribed to be the same as $d_c$, i.e., 30 $\mu$m.

### D. Mechanical Robustness

Because the inductors were suspended, mechanical robustness must be considered. Since the spiral is composed of many strips, we investigated this issue starting with a simple beam. Given a cantilever beam with a length of $L_b$, a width of $W_b$, and a thickness of $T_b$, the stiffness constant $k$ in the direction of $T_b$ is given by

$$k = \frac{EW_bT_b^3}{4L_b^3} \tag{1}$$

where $E$ is the Young's modulus. Permutation of $L_b$, $W_b$, and $T_b$ in (1) gives the stiffness constants of the beam in the directions of $W_b$ and $L_b$ as well. If $L_b > W_b > T_b$, which is true in our structures, the beam is most prone to bending in the direction of $T_b$, and $k$ calculated in (1) is the smallest among the three stiffness constants. For a worst case study, we will use $k$ given in (1).

Because the Young's modulus of Cu is 130 GPa [23], very close to that of polysilicon, which is approximately 150 GPa [24], the difference between the Young's moduli of these two materials can be neglected when we study the mechanical property of the inductors. Cu itself, however, is not suitable as the structural material because its yield strength, approximately 0.26 GPa [25], is considerably lower than that of silicon, which is about 7.0 GPa [17]. An estimation of $k$ can then be calculated by assuming $E \approx 150$ GPa, $W_b \approx 15$ $\mu$m, $L_b \approx 200$ $\mu$m, and $T_b \approx 3.5$ $\mu$m, including 1.5 $\mu$m of polysilicon and 1 $\mu$m of Cu at each side of the strip, which yields that $k \approx 3$ $\mu$N/$\mu$m.

The mass of the inductor is given by

$$m = (2\rho_c t + \rho_s t_s)L_{\rm tot} w$$

where $\rho_s$ is the density of polysilicon, which is 2.33 g/cm$^3$ [24]; $\rho_c$ is the density of Cu, which is 8.94 g/cm$^3$ [23]; and $L_{\rm tot}$ is the total length of the polysilicon strips of the spiral. The mass $m$ can be reasonably estimated by assuming $L_{\rm tot} \approx 5$ mm and, again, $w \approx 15$ $\mu$m, $t \approx 1$ $\mu$m, and $t_s \approx 1.5$ $\mu$m, which yields that $m \approx 1.6$ $\mu$g. Suppose the device undergoes a shock that amounts to an acceleration $a = 20$ g, where "g" is the gravitational acceleration, or 9.8 m/s$^2$. The virtual force experienced by the device is $F = ma \approx 0.3$ $\mu$N. Such a force will cause a strip to bend by $b = F/k \approx 0.1$ $\mu$m. Since the above calculation is conservative, as long as the dimensions of the spiral, especially the thickness of and the spacing between the strips, are kept much larger than 0.1 $\mu$m, the change in the geometry of the inductor, and thus in its characteristics such as inductance, will be negligible.

Another figure of merit is the mechanical resonant frequency of the inductor $f_R$, which can be roughly calculated by

$$f_R = \frac{1}{2\pi}\sqrt{\frac{k}{m}}.$$

Using the values already obtained, we find $f_R \approx 7$ kHz. Given that the environmental vibrations are generally much smaller than 1 kHz, such vibration should not affect the inductor.

### E. Design of Overpasses

In our structures, the overpasses mechanically suspend the inductor spirals. The critical issue in the design of overpasses,

therefore, rests in the vias that connect the overpasses and the spiral. To ensure good connection, large 10 $\mu$m $\times$ 10 $\mu$m vias were used. As a result, the width of the overpasses $w_o$ was designed to be 18 $\mu$m, leaving room for alignment tolerance during the process. As already shown in the discussion above, this width is sufficient for a reasonably large shock.

## IV. Characterization

After the fabrication of the inductors, on-wafer testing was performed with an HP8510C network analyzer and PI-COPROBE coplanar ground–signal–ground (GSG) probes. We deembedded the shunt parasitics due to the testing pads using open pads next to the device under test (DUT) [26]. The two-port circuit parameters were then converted from the measured $S$-parameters.

One approach to studying the behavior of the inductors is to utilize a simplified equivalent circuit model composed of a few lumped elements, typically including an inductor, a series resistor, and a few capacitors and resistors to account for the substrate coupling and loss [1], [4], [10], [27], [28]. Due to the oversimplicity of these models, more complicated ones are proposed for the better understanding of the inductors [26], [29]. Because of the peculiarity of our structure, especially the influence of the cavity beneath the inductor, the extraction method of $Q$ should be model independent. We first applied the conventional definition of $Q$ as given in [1]

$$Q_{\rm conv} = -\frac{{\rm Im}(Y_{11})}{{\rm Re}(Y_{11})}$$

where $Y_{11}$ is the short-circuit input admittance of the inductor. This definition has an undesirable characteristic that $Q$ drops to zero at $f_{\rm res}$, which can be understood by studying the tantamount definition in [30]

$$Q_{\rm conv} = 2\omega\frac{(|\overline{W_m}| - |\overline{W_e}|)}{P_{\rm diss}}$$

where $\overline{W_m}$ and $\overline{W_e}$ are the average magnetic and electric energy stored in the inductor and $P_{\rm diss}$ is the power dissipation. The original definition of $Q$, $Q_{\rm real}$, given in

$$Q_{\rm real} = 2\omega\frac{(|\overline{W_m}| + |\overline{W_e}|)}{P_{\rm diss}}$$

should be applied instead. Hence, at $f_{\rm res}$, where $\overline{W_m}$ equals $\overline{W_e}$, $Q_{\rm conv}$ gives zero but $Q_{\rm real}$ is much larger. In order to get a better picture of the performance of the inductor near $f_{\rm res}$, we took a more application-oriented approach. In this method, an ideal capacitor is numerically inserted in shunt with the inductor. By scanning the capacitance of this ideal capacitor, the resonant frequency $f_0$ of the device will be swept as well [31]. At each $f_0$, a 3-dB bandwidth $\Delta f_{\rm 3dB}$ can be obtained by studying the short-circuit current transfer function of the new device (see the inset of Fig. 11) $-H'_{21}$. $Q_{\rm 3dB}$ can then be defined as in [14]

$$Q_{\rm 3dB} = \frac{\omega_0}{\Delta\omega_{\rm 3dB}}.$$

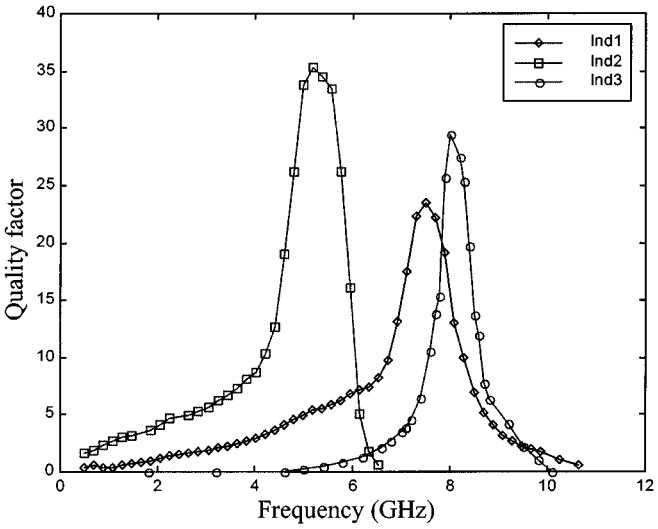


Fig. 10. Measured $Q$-factors by the conventional definition.

TABLE III
Measured $Q_{\rm max}$, $f_{\rm max}$, and $f_{\rm res}$

| | *Ind1* | *Ind2* | *Ind3* |
|---|---|---|---|
| $Q_{max}$ | 23 | 36 | 30 |
| $f_{max}$ (GHz) | 7.5 | 5.2 | 8.0 |
| $f_{res}$ (GHz) | 10.7 | 6.6 | 10.1 |

Equally feasible, by examining the rate of change in phase of the new device's $Y_{11}$, another equivalent quality factor $Q_{\rm pha}$ can be found from [31]

$$\left.\frac{d\phi}{d\omega}\right|_{\omega_0} = \frac{2Q_{\rm pha}}{\omega_0} = \frac{\angle Y'(\omega_0+\delta\omega) - \angle Y'(\omega_0-\delta\omega)}{2\delta\omega}.$$

These two definitions of $Q$ are more suitable in evaluating the performance of an inductor when it is used in circuits such as bandpass filters and equalizers.

Fig. 10 shows $Q_{\rm conv}$ of the three inductors versus frequency. Table III itemizes $Q_{\rm max}$, the measured maximum $Q$, $f_{\rm max}$, the frequency at which $Q$ reaches the maximum, and $f_{\rm res}$, where ${\rm Im}(Y_{11})$ becomes zero, for each of the inductors. As demonstrated, $Q$ as high as 36 and $f_{\rm res}$ as high as 10.7 GHz have been achieved. $Q$ of *Ind1* is notably lower, probably due to its narrower strips. We have also applied the other two definitions of $Q$, $Q_{\rm 3dB}$ and $Q_{\rm pha}$ to *Ind2* as an example. As shown in Fig. 11 [14], the maximum of $Q_{\rm 3dB}$ reaches a high 84 and that of $Q_{\rm pha}$ 46. At the $f_{\rm res}$ of 6.6 GHz, when the capacitance of the added ideal capacitor is zero, $Q_{\rm 3dB}$ and $Q_{\rm pha}$ remain larger than ten, indicating still good performance. It should be pointed out that by adding the ideal capacitor, energy stored in it would be introduced into the total energy in the two elements while the power dissipation is still only due to the inductor. This accounts for the much larger $Q_{\rm max}$ observed than the conventional definition at frequencies other than $f_{\rm res}$. However, as figures of merit, these two $Q$s indicate the maximum performance accomplishable for a circuit that incorporates the given inductor [30].

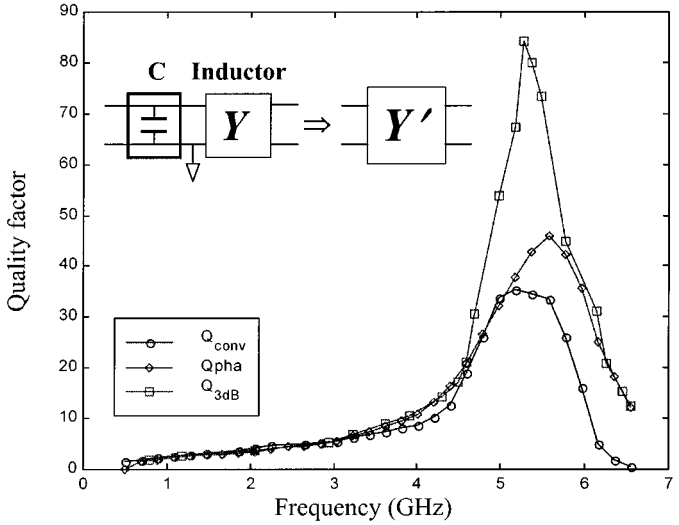


Fig. 11. $Q$-factors of *Ind2* by different definitions [14].

## V. Conclusion

We have developed and employed a silicon micromachining fabrication method to build monolithically on silicon high-performance on-chip spiral inductors. The devices were constructed using two-layer polysilicon micromachining and were suspended over 30-$\mu$m-deep cavities formed in the silicon substrate. Electroless Cu plating was performed to metallize the polysilicon device structures for low series resistance. The same Cu deposition process coated the inner surfaces of the cavities, which formed good RF ground, and electric and magnetic shielding. The deep cavities diminish the electric and magnetic coupling, and the parasitic capacitances between the devices and the silicon substrate. $Q$-factor over 30 and $f_{\rm res}$ higher than 10 GHz have been demonstrated. Mutual inductance between a pair of identical inductors placed 25 $\mu$m apart drops by as much as a factor of 20 to a few picohenries with the Cu-lined cavities, compared with that with silicon substrate 2 $\mu$m beneath. Consequently, the magnetic coupling among inductors is reduced significantly, and so will be the crosstalk. This fabrication method can be extended to make other high-performance on-chip passive components, such as tunable parallel-plate capacitors and transformers [32], for more extensive applications. It can potentially be integrated with conventional CMOS technologies as well.

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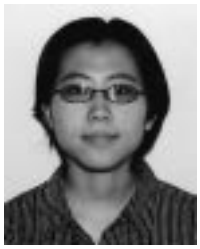

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