A UNIVERSAL MEMS FABRICATION PROCESS FOR HIGH-PERFORMANCE ON-CHIP RF PASSIVE COMPONENTS AND CIRCUITS

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ABSTRACT

We have developed a fabrication approach that allows us to integrate monolithically on silicon high-performance on-chip radio-frequency (RF) passive components, such as inductors, transformers and fixed and tunable capacitors. We applied two-layer polysilicon surface micromachining to construct the devices, which were suspended over 30-μm-deep cavities formed into the silicon substrate. We also performed electroless copper (Cu) plating to metallize the polysilicon structures for high conductivity. The inner surfaces of the cavities were Cu coated too, providing good RF ground and electromagnetic shielding. The deep cavities dramatically reduce the electric and magnetic couplings and parasitic capacitances between the devices and the substrate. High quality factors over 30 and resonant frequencies over 10 GHz have been achieved for inductors. We have designed and fabricated high-performance varactors, transformers and *LC*-passive filters as well.

INTRODUCTION

On-chip passive components, such as inductors, capacitors, and transformers are indispensible in radio-frequency (RF) circuits for wireless communication **[1-2]**. Today's on-chip inductors, however, generally have low quality factors (Q's), lack good RF grounds, have characteristics dependent on the substrate geometry and their ambient due to electromagnetic coupling, and have low self-resonant frequencies. Many techniques have been developed to reduce the substrate loss and/or parasitics between the inductors and the substrate, such as using a high-resistivity silicon substrate, silicon on sapphire, glass or quartz, etching away the substrate under the device **[3]**, and building the inductor on a thick silicon-oxide layer **[4]**. These methods, however, cannot solve the ground and cross-talk problems. To provide an electromagnetic shield, a patterned metal shield can be inserted beneath the inductor **[3]**, but the benefit is counterbalanced, more or less, by the loss induced within the inserted shield itself. These problems also apply to on-chip transformers. Tunable capacitors have also been reported using two metal layers **[5]** or two polysilicon layers **[6]**. Because the metal used is soft, it cannot form large-area suspended plates. Therefore, the capacitances achieved are small and multiple capacitors must be put in parallel to reach values of a few picofarads **[5]**, which are commonly used in RF circuits. With polysilicon plates, on the other hand, only the top polysilicon layer can be metallized **[6]**, which produces a large series resistance for the capacitor and low Q. Another issue stems from the closeness between the capacitor plates and the silicon substrate, which creates a large parasitic capacitance, on the same order of magnitude as the capacitance obtained from the parallel plates. Consequently, the tunable range of such a varactor is very small **[5]**. This will be a severe problem for a floating capacitor, which is commonly used. Moreover, these disparate approaches cannot simultaneously solve all the problems involved in the optimization of the elements discussed, let alone provide for the integration of various elements on one chip **[3-7]**.

We previously reported a microelectromechanical-system (MEMS) technology to create on-chip high-Q suspended electromagnetically-shielded spiral inductors, using silicon micromachining and electroless copper (Cu) plating **[8-9]**. We have improved and extended this process to a universal one with which we can integrate most of the high-performance RF passive components just mentioned onto a silicon substrate. Circuits such as low-pass filters are also realizable through this method. The fabrication processes are also CMOS-compatible; therefore, it can potentially be integrated with CMOS technologies for wider applications.

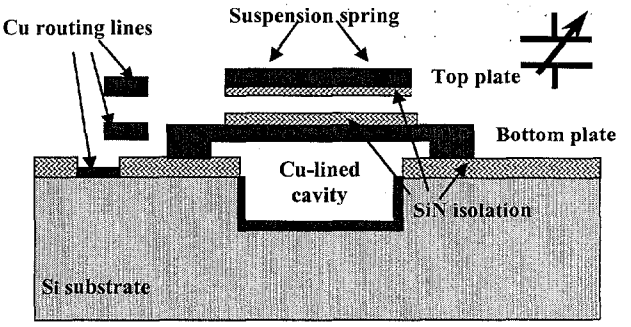


Figure 1. Schematic of the cross section of an electrostatically actuated parallel-plate varactor.

PRINCIPLE AND DESIGN

Our approach features the suspension of all of the devices over cavities formed in the silicon substrate and conformal encapsulation of selectively exposed silicon and polysilicon structures with Cu. The cavity, currently chosen to be 30-μm deep, dramatically reduces the electromagnetic coupling and the parasitic capacitance between the device and the substrate. To save die area, the cavity has vertical sidewalls and an opening slightly larger than the device. Polysilicon is used as the structural material of the suspended devices. The choice of polysilicon as the structural material is based on two factors. First, polysilicon is a stiff material **[10]** that can well withstand vibrations and shocks from the environment. Second, polysilicon surface micromachining is well developed and has the flexibility to produce complex structures **[11]**. Cu encapsulation of the polysilicon structures renders low resistance comparable to metal. The cavities beneath the devices are lined with Cu in the same plating procedure to provide both good RF ground and electromagnetic shielding that isolates the devices from their ambient. Hence, high device performances can be achieved in terms of high Q, good isolation, and, in the varactor's case, large tunability. Figure 1 shows schematically the cross section of a parallel-plate varactor fabricated by this method.

FABRICATION PROCESS

The fabrication process was carried out at the Cornell Nanofabrication Facility (CNF). The schematic of the process flow is shown in Figure 2, where the manufacture of a tunable capacitor is used as an example. The process started with the deposition of an 800-nm-thick low-pressure chemical vapor-deposited (LPCVD)

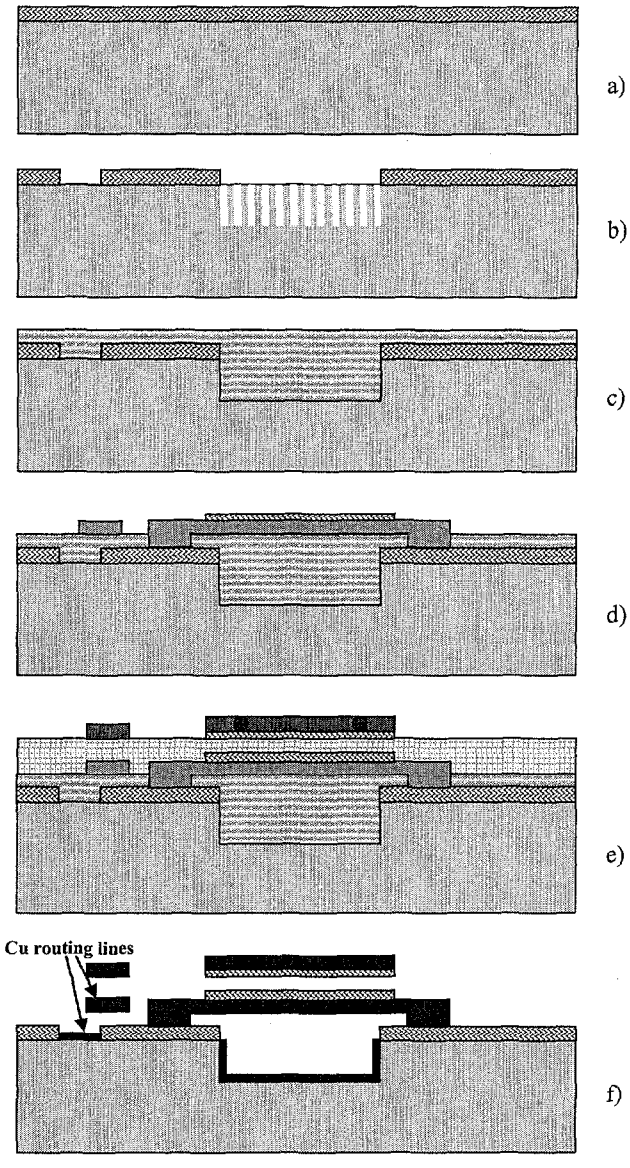


Figure 2. *Schematic of the process flow: a) deposition and patterning of isolation silicon nitride; b) etching narrow beam-and-trench structures for the sacrificial silicon-oxide block by DRIE; c) thermal oxidation, silicon-oxide deposition and CMP to form the sacrificial block; d) deposition and patterning of the first polysilicon structural and silicon-nitride isolation layers; e) deposition and patterning of the second sacrificial silicon oxide, the second polysilicon structural and silicon-nitride isolation layers; f) HF release, RTA and electroless Cu plating.*

low-stress silicon-nitride film as the isolation layer (Figure 2a). Then, the areas where the sacrificial silicon-oxide blocks for the cavity formation were to be defined were opened by etching away the silicon-nitride layer. The patterns of the first-level Cu routing lines were etched out as well in this step. Next, 30-μm-deep narrow beam-and-trench structureswere created in those opened windows for the sacrificial silicon-oxide blocks by deep reactive ion etching (DRIE) (Figure 2b). Afterwards, the narrow beams were thermally oxidized, followed by the deposition of an LPCVD low-temperature oxide (LTO) to completely seal any openings or gaps left after the thermal oxidation. The SEM image of the cross section of a silicon-oxide block thus formed is shown in Figure 3, where the ripples on the surface due to the sealing of the openings

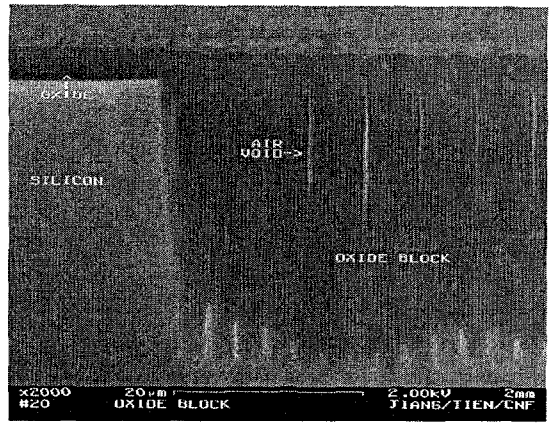


Figure 3. *SEM image of the cross section of a 30-μm-deep sacrificial silicon-oxide block.*

are clearly shown. Chemical mechanical polishing (CMP) was applied to provide a flat surface for the later steps (Figure 2c).

After the formation of the sacrificial silicon-oxide block, a two-polysilicon-layer surface micromachining process was applied to build the devices. These two n-type polysilicon layers were doped *in situ* using phosphine (PH_3) as the phosphorus source. The first polysilicon film was used to form the following structures: the inductor spirals, the transformer coils, the bottom plates of the capacitors and the second-level Cu wirings (Figure 2d). The second polysilicon layer was employed to build the following: the overpasses of the inductors, the transformer coils, if necessary, the top plates of the capacitors, the suspension springs of the variable capacitors and the third-level Cu wirings (Figure 2e). The function of the overpasses of the inductors is to connect the input and output ports across the spiral traces and the cavity edges to probing pads outside. A second LPCVD LTO sacrificial layer of a thickness of 3.2 μm was grown and separated the polysilicon layers. This silicon-oxide film was planarized and thinned by a second CMP step. Its thickness was determined by the designed air gap between the two plates of the variable capacitors, which was 1.2 μm in this run. Two thin 250-nm-thick LPCVD low-stress silicon-nitride films were grown and lithographically patterned, one onto the first polysilicon layer and the second onto the second sacrificial silicon-oxide layer, immediately under the second polysilicon layer, wherever overlapping or crossover between the two polysilicon layers occurred. These two silicon-nitride films served as isolation and Cu-plating stoppage layers, because it was found that the electroless Cu deposition favored the areas where the structures were dense, which might cause shorting problems **[9]**. These two silicon-nitride layers were also used as the dielectric materials between the two plates of fixed capacitors.

The post-processing began with a rapid thermal annealing (RTA) step at the temperature of 1100 °C for 90 seconds to relieve the internal and interfacial stress. The structures were finally released in hydrofluoric (HF) acid and electroless Cu plating was performed (Figure 2f). The process was selective: all the exposed silicon and polysilicon structures were plated with Cu, including the inductors, transformers, capacitors and metal routing lines, while those structures covered with silicon nitride remained as they were, providing good isolation. Figure 4 shows the focus-ion-beam (FIB) image of the cross section of a polysilicon coil fully encapsulated with Cu. As is clearly demonstrated, the plating is conformal. The resistivity of the plated Cu was measured to be 2.1 μΩ-cm **[9]**.

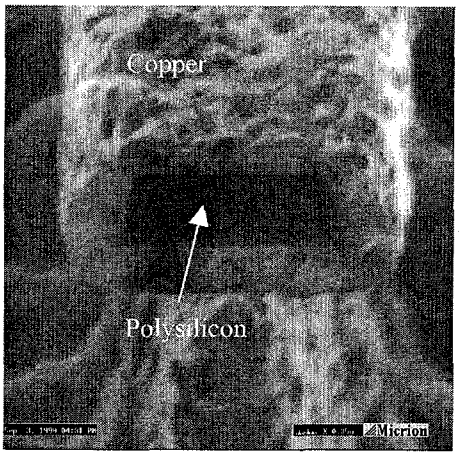
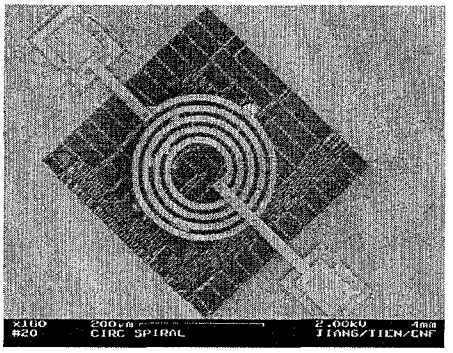


***Figure 4**. Focus ion beam micrograph of the cross section of a polysilicon coil encapsulated with Cu [9].*



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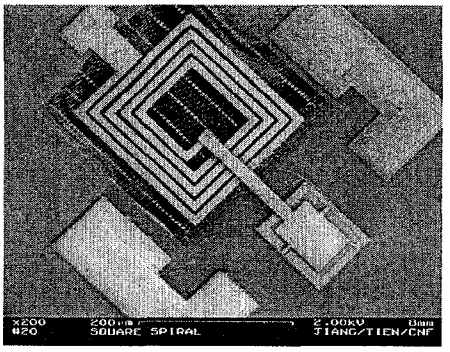


b)

***Figure 5**. SEM image of spiral suspended inductors: a) circular and b) rectangular.*

TEST DEVICES

Figure 5 shows the SEM images of suspended spiral inductors, in both circular (Figure 5a) and rectangular shapes (Figure 5b). The fabricated inductors have inductances ranging from about 1 nH to about 10 nH, and occupy areas, including the cavities beneath, from about 150 × 150 μm^2 to about 350 × 350 μm^2. High Q over 30 and self-resonance frequency above 10 GHz have been accomplished **[8-9]**. Circular spirals suffer less bending and warping after HF release than rectangular ones, probably because the right-angle corners of the rectangular spirals have more stress. Nevertheless, rectangular inductors are studied more comprehensively because they are easier to simulate in a finite-element-method (FEM) simulator such as Microcosm MEMCAD. Simulation predicts that, owing to the Cu-lined cavity, the mutual inductance between two adjacent inductors drops by a factor around 5 from that without the cavity **[9]**, indicating good shielding effect.

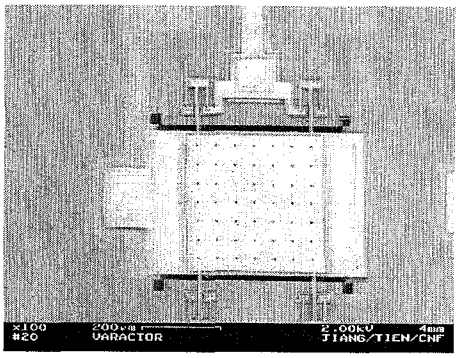
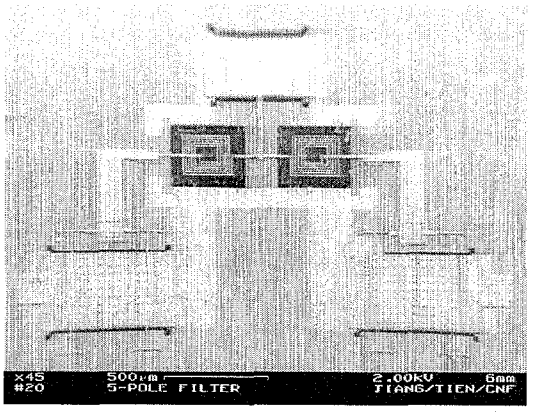


***Figure 6**. SEM image of an electrostatically actuated parallel-plate tunable capacitor.*

Figure 6 shows an electrostatically actuated parallel-plate varactor. The overlapping area of the two plates are 400 × 400 μm^2 and the air gap between them is 1.2 μm, which gives a nominal capacitance of 1.1 pF if no DC voltage is applied across the two plates. The nominal tunability of this varactor is close to 1.5:1, the maximum predicted by theory **[6]**, owing to the negligible parasitic capacitance between the plates and the cavity inner surfaces. With the designed total spring constant of 4.3 N/m, the maximum capacitance can be achieved under the maximum bias of 3 V.



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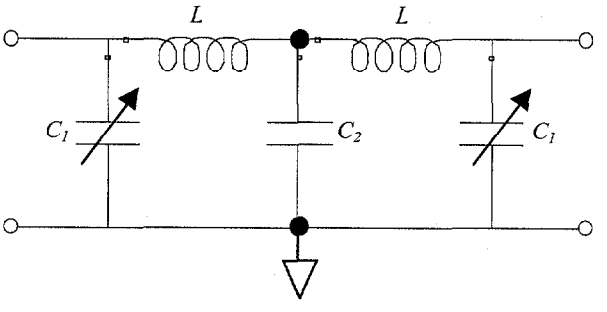
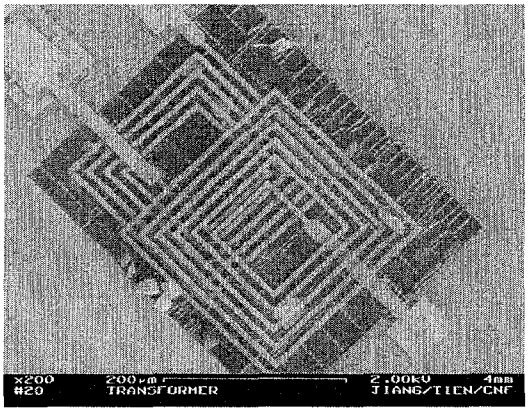


b)

***Figure 7**. a) SEM image of a five-pole tunable low-pass LC-ladder filter and b) its simplified circuit diagram.*

Passive LC-filters can be built incorporating the inductors and capacitors described above. A prototype five-pole tunable low-

pass *LC*-ladder filter was fabricated and is demonstrated in Figure 7a and its simplified circuit diagram is given in Figure 7b. The filter consists of two inductors (Figure 7a middle) with nominal inductances of 8 nH, two varactors (Figure 7a bottom) with nominal capacitances varying from 1.1 to 1.65 pF, and one fixed capacitor (Figure 7a top) with nominal capacitance of 10 pF. Simulation predicts a 3-dB frequency ranging from 800 to 900 MHz and a roll-off slope of 30 dB/octave.



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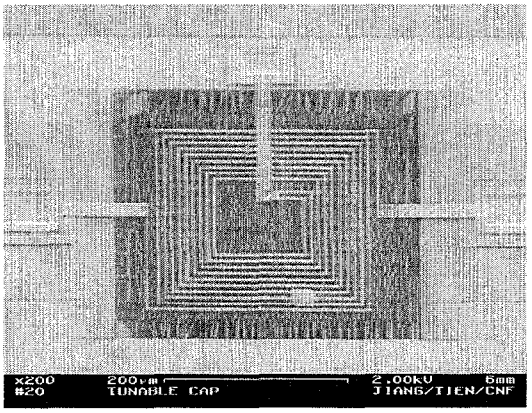

b)

Figure 8. *SEM images of a) a stacked and b) an interleaved three-terminal transformer.*

Figure 8 gives two configurations, stacked (Figure 8a) and interleaved (Figure 8b), of three-terminal transformers. The stacked one is composed of two overlapping spirals built in two polysilicon layers. An overpass and an underpass, respectively, are needed to tap the centers of the coils to outside, as in the case of inductors, and are also made out of the polysilicon. The parameters of these two transformers at 2 GHz, the self-inductances of the primary and secondary coils, L_{pri} and L_{sec}, the mutual inductance, M, and the coupling coefficient, k, defined by $k = M / \sqrt{L_{pri} L_{\sec}}$, were simulated by ASITIC **[12]** and are listed in Table 1. The interleaved configuration offers a large coupling coefficient, k, between the primary and secondary coils, while the stacked structure provides a lower k. This phenomenon is due to the restriction on the overlap area between the two coils to avoid the touching of the overpass/underpass and the coils. Nonetheless, the stacked configuration offers flexibility in k because it allows varying overlap between the primary and secondary coils.

Table 1. *Simulated parameters of transformers at 2 GHz.*

	L_{pri} (nH)	L_{sec} (nH)	M	k
stacked	7.0	6.2	2.1	0.32
interleaved	6.0	5.6	4.6	0.79

CONCLUSION

We have developed and employed a universal MEMS fabrication method to build monolithically on silicon high-performance on-chip passive components, including inductors, transformers and electrostatically actuated parallel-plate tunable capacitors. The devices were constructed using two-layer polysilicon micromachining and were suspended over 30-μm-deep cavities formed in the silicon substrate. Electroless Cu plating was performed to metallize the polysilicon device structures for low series resistance. The same Cu deposition process coated the inner surfaces of the cavities, which formed good RF ground and electric and magnetic shielding. The deep cavities diminish the electric and magnetic couplings and the parasitic capacitances between the devices and the silicon substrate. Therefore, high Q's and small cross-talks for the devices, high self-resonant frequencies for the inductors and large tunability of 1.5:1 for varactors, respectively, can be achieved. An *LC*-ladder filter was designed and fabricated as well. The process can be potentially integrated with conventional CMOS technologies for wider applications.

ACKNOWLEDGEMENTS

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